

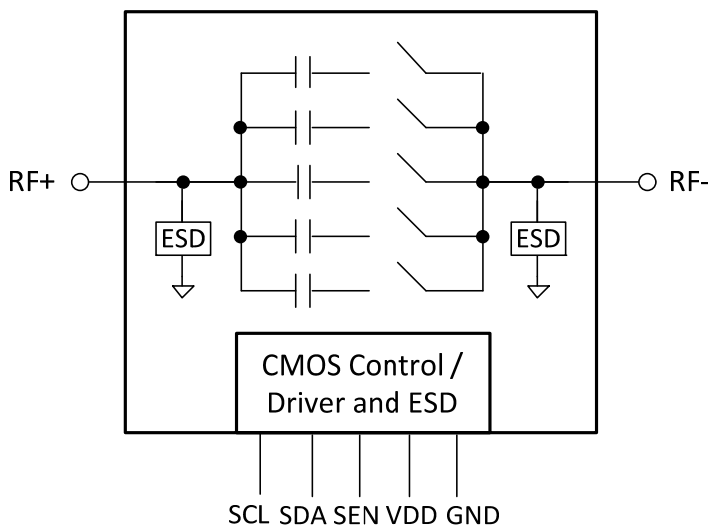
**Product Description**

PE623080 is a DuNE™-enhanced Digitally Tunable Capacitor (DTC) based on Peregrine’s UltraCMOS® technology. This highly versatile product supports a wide variety of tuning circuit topologies with emphasis on impedance matching and aperture tuning applications. PE623080 is optimized for key cellular frequency bands from 700 to 2700 MHz.

PE623080 offers high RF power handling and ruggedness while meeting challenging harmonic and linearity requirements enabled by Peregrine’s HaRP™ technology. The device is controlled through the widely supported 3-wire (SPI compatible) interface. All decoding and biasing is integrated on-chip and no external bypassing or filtering components are required.

DuNE™ devices feature ease of use while delivering superior RF performance in the form of tuning accuracy, monotonicity, tuning ratio, power handling, size, and quality factor. With built-in bias voltage generation and ESD protection, DTC products provide a monolithically integrated tuning solution for demanding RF applications.

**Figure 1. Functional Block Diagram**



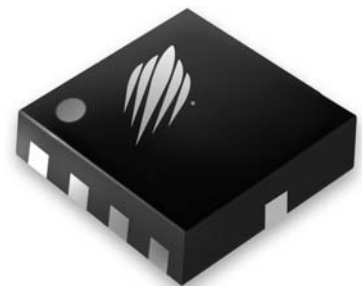
**UltraCMOS® Digitally Tunable Capacitor (DTC) Optimized for 2G/3G/4G Tuning Applications, 100-3000 MHz**

**Features**

- 5-bit 32-state Digitally Tunable Capacitor
- Shunt configuration  $C = 2.15 - 7.7 \text{ pF}$  (3.6:1 tuning ratio) in discrete 180 fF steps
- High RF power handling (30  $V_{pk}$  RF) and linearity for 2G/3G/4G applications
- Wide power supply range (2.3 to 4.8V) for operation from  $V_{BATT}$
- 2 x 2 x 0.55 mm QFN package
- High ESD tolerance of 2kV HBM on all pins
- Applications include:
  - Open and closed-loop Tunable Antennas for 2G/3G/4G
  - Tunable Matching Networks
  - Tunable Filter Networks

**Figure 2. Package Type**

10-lead 2 x 2 x 0.55 mm QFN package



**Table 1. Electrical Specifications @ 25 °C, V<sub>DD</sub> = 2.75V  
(In shunt configuration between 50 Ω ports, RF- connected to GND)**

Parameter	Condition	Min	Typ	Max	Unit
Operating Frequency Range		100		3000	MHz
Minimum Capacitance	State 00000, 100 MHz	1.93	2.15	2.37	pF
Maximum Capacitance	State 11111, 100 MHz	6.93	7.70	8.47	pF
Tuning Ratio	C <sub>max</sub> /C <sub>min</sub> , 100 MHz		3.6:1		
Step Size	5 bits (32 states), 100 MHz		0.180		pF
Quality Factor (C <sub>min</sub> ) <sup>1</sup>	698-960 MHz, with L <sub>S</sub> removed 1710-2170 MHz, with L <sub>S</sub> removed		41 24		
Quality Factor (C <sub>max</sub> ) <sup>1</sup>	698-960 MHz, with L <sub>S</sub> removed 1710-2170 MHz, with L <sub>S</sub> removed		15 6		
Self Resonant Frequency <sup>5</sup>	State 00000 State 11111		3.9 2.1		GHz
Harmonics <sup>2</sup>	2fo: 698 to 915 MHz; Pin +34 dBm, 50 Ω 3fo: 698 to 915 MHz; Pin +34 dBm, 50 Ω 2fo: 1710 to 1910 MHz; Pin +32 dBm, 50 Ω 3fo: 1710 to 1910 MHz; Pin +32 dBm, 50 Ω		-40 -50 -40 -50	-36 -36 -36 -36	dBm dBm dBm dBm
IMD3	Bands I,II,V/VIII, +20 dBm CW @ TX freq, -15 dBm CW @ 2Tx-Rx freq, 50 Ω		-115	-105	dBm
Switching Time <sup>3,4</sup>	State change to 10/90% delta capacitance between any two states			12	µs
Start-up Time <sup>3</sup>	Time from V <sub>DD</sub> within specification to all performances within specification			70	µs
Wake-up Time <sup>3,4</sup>	State change from Standby mode to RF state to all performances within specification			70	µs

- Notes: 1. Q for a Shunt DTC based on a Series RLC equivalent circuit  
 $Q = X_C/R = (X-X_L)/R$ , where  $X = X_L+X_C$ ,  $X_L = 2\pi fL$ ,  $X_C = -1/(2\pi fC)$ , which is equal to removing the effect of parasitic inductance L<sub>S</sub>  
 2. In Shunt between 50 Ω ports. Pulsed RF input with 4620 µS period, 50% duty cycle, measured per 3GPP TS 45.005  
 3. DC path to ground at RF- must be provided to achieve specified performance  
 4. State change activated on falling edge of SEN following data word  
 5. DTC operation above SRF is possible

Figure 3. Pin Configuration (Top View)

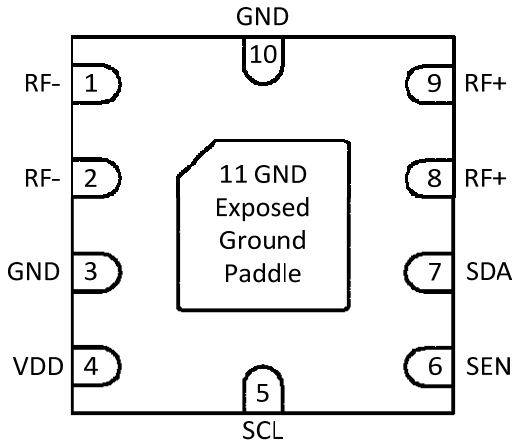


Table 2. Pin Descriptions

Pin #	Pin Name	Description
1	RF-	Negative RF Port <sup>1</sup>
2	RF-	Negative RF Port <sup>1</sup>
3	GND	Ground <sup>2</sup>
4	V <sub>DD</sub>	Supply
5	SCL	Serial Interface Clock Input
6	SEN	Serial Interface Latch Enable Input
7	SDA	Serial Interface Data Input
8	RF+	Positive RF Port <sup>1</sup>
9	RF+	Positive RF Port <sup>1</sup>
10	GND	Ground <sup>2</sup>
11	GND	Exposed Ground Paddle <sup>2</sup>

Notes: 1. Multiple RF pins are provided for flexibility. They can be tied together for optimal RF performance, or used individually (leave unused pin floating)  
 2. For optimal performance, recommend tying Pins 3, 10, and 11 together on PCB

### Moisture Sensitivity Level

The Moisture Sensitivity Level rating for the PE623080 in the 10-lead 2 x 2 x 0.55 mm QFN package is MSL1.

Table 3. Operating Ranges

Parameter	Min	Typ	Max	Unit
V <sub>DD</sub> Supply Voltage	2.30	2.75	4.80	V
I <sub>DD</sub> Power Supply Current (V <sub>DD</sub> = 2.75 V)		140	200	μA
I <sub>DD</sub> Standby Current (V <sub>DD</sub> = 2.75 V)		25		μA
V <sub>IH</sub> Control Voltage High	1.2	1.8	3.1	V
V <sub>IL</sub> Control Voltage Low	0	0	0.57	V
RF Input Power (50 Ω) <sup>1</sup> 698 to 915 MHz 1710 to 1910 MHz			+34 +32	dBm dBm
Peak Operating RF Voltage <sup>2</sup> V <sub>P</sub> to V <sub>M</sub> V <sub>P</sub> to RFGND			30 30	V <sub>pk</sub> V <sub>pk</sub>
T <sub>OP</sub> Operating Temperature Range	-40	+25	+85	°C
T <sub>ST</sub> Storage Temperature Range	-65	+25	+150	°C

Notes: 1. Maximum power available from 50 Ω source. Pulsed RF input with 4620 μs period, 50% duty cycle, measured per 3GPP TS 45.005 measured in shunt between 50 Ω ports, RF- connected to GND  
 2. Node voltages defined per Equivalent Circuit Model Schematic (Figure 12). Refer to page 7 if using DTC in series configuration

Table 4. Absolute Maximum Ratings

Symbol	Parameter/Conditions	Min	Max	Unit
V <sub>ESD</sub>	ESD Voltage (HBM, MIL_STD 883 Method 3015.7)		2000	V

Exceeding absolute maximum ratings may cause permanent damage. Operation should be restricted to the limits in the Operating Ranges table. Operation between operating range maximum and absolute maximum for extended periods may reduce reliability.

### Electrostatic Discharge (ESD) Precautions

When handling this UltraCMOS<sup>®</sup> device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the specified rating.

### Latch-Up Avoidance

Unlike conventional CMOS devices, UltraCMOS<sup>®</sup> devices are immune to latch-up.

Performance Plots @ 25°C and 2.75V unless otherwise specified

Figure 4. Measured Shunt C (@ 100 MHz) vs State

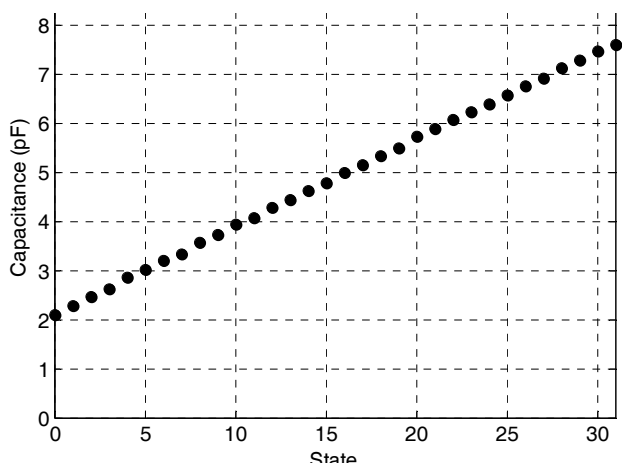


Figure 5. Measured Shunt S<sub>11</sub> (major states)

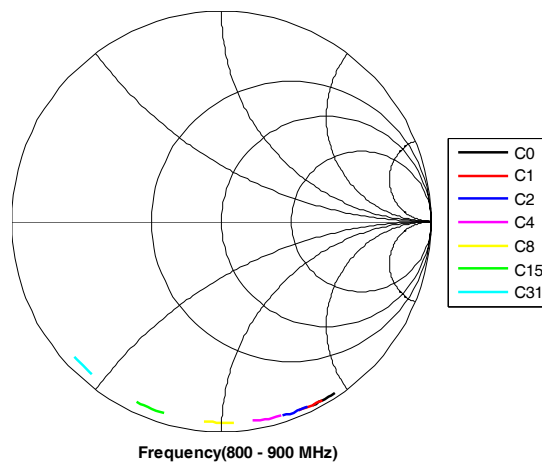


Figure 6. Measured Step Size vs State (frequency)

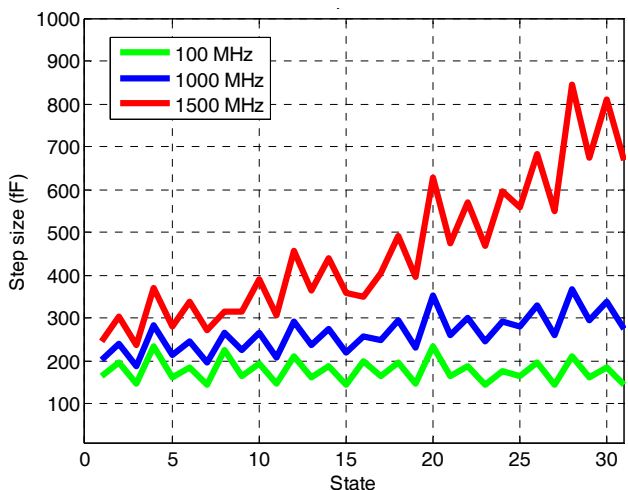


Figure 7. Measured Shunt C vs Frequency (major states)

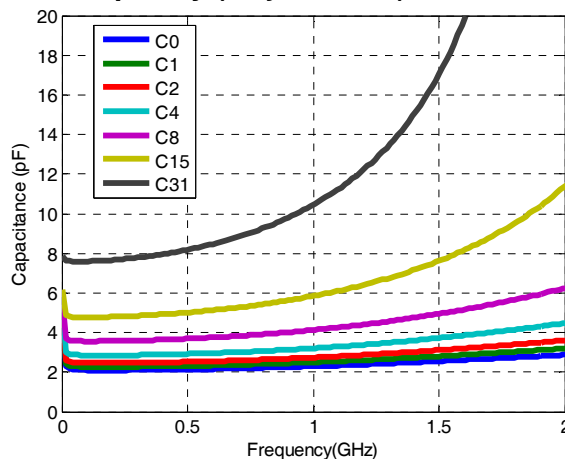


Figure 8. Measured Shunt Q vs Frequency (major states)

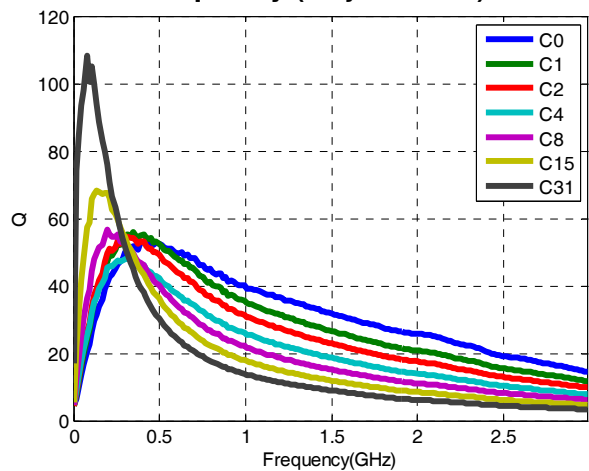
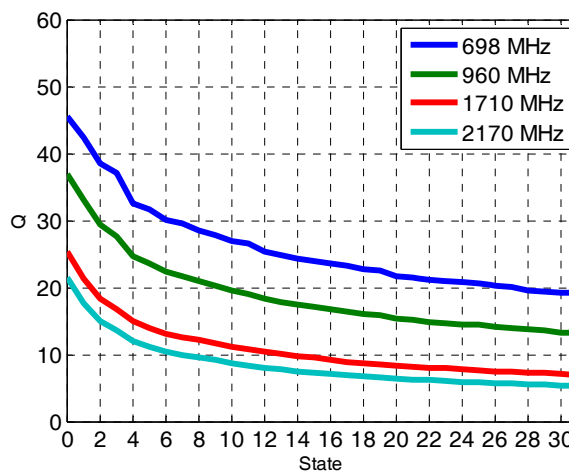


Figure 9. Measured Shunt Q vs State



### Serial Interface Operation and Sharing

The PE623080 is controlled by a three wire SPI-compatible interface with enable active high. As shown in *Figure 10*, the serial master initiates the start of a telegram by driving the SEN (Serial Enable) line high. Each bit of the 8-bit telegram (MSB first in) is clocked in on the rising edge of SCL (Serial Clock), as shown in *Table 5* and *Figure 10*. Transitions on SDA (Serial Data) are allowed on the falling edge of SCL. The DTC activates the data on the falling edge of SEN. The DTC does not count how many bits are clocked and only maintains the last 8 bits it received.

More than 1 DTC can be controlled by one interface by utilizing a dedicated enable (SEN) line for each DTC. SDA, SCL, and V<sub>DD</sub> lines may be shared as shown in *Figure 11*. Dedicated SEN lines act as a chip select such that each DTC will only respond to serial transactions intended for them. This makes each DTC change states sequentially as they are programmed.

Alternatively, a dedicated SDA line with common SEN can be used. This allows all DTCs to change states simultaneously, but requires all DTCs to be programmed even if the state is not changed.

Figure 10. Serial Interface Timing Diagram

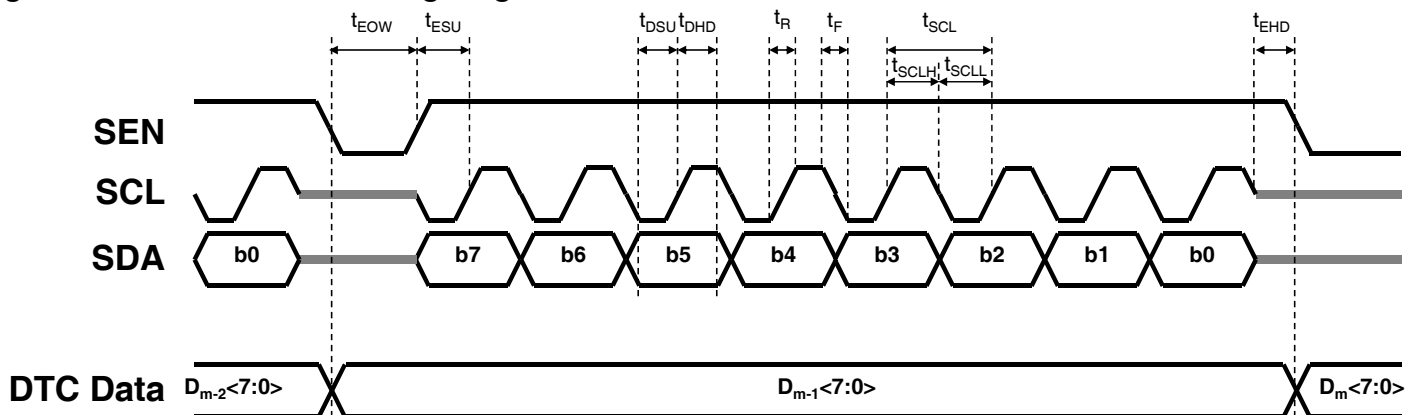


Table 5. 8-Bit Serial Programming Register Map

b7	b6	b5	b4	b3	b2	b1	b0
0 <sup>1</sup>	0 <sup>1</sup>	STB <sup>2</sup>	d4	d3	d2	d1	d0

MSB (first in)

LSB (last in)

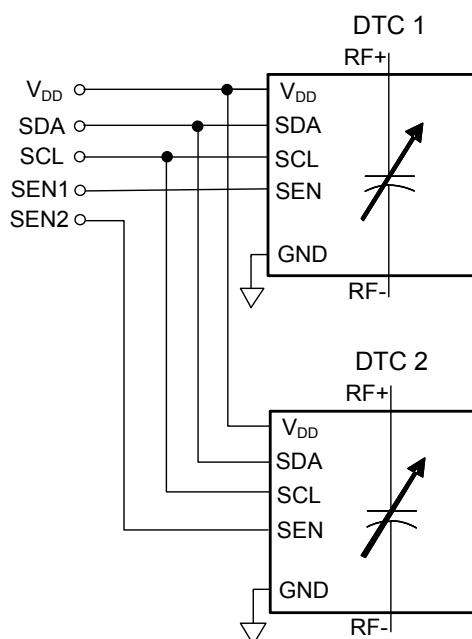
- Notes: 1. These bits are reserved and must be written to 0 for proper operation  
 2. The DTC is active when low (set to 0) and in low-current stand-by mode when high (set to 1)

Table 6. Serial Interface Timing Characteristics

V<sub>DD</sub> = 2.75V, -40 °C < T<sub>A</sub> < +85 °C, unless otherwise specified

Symbol	Parameter	Min	Max	Unit
t <sub>SCL</sub>	Serial Clock Period	38.4		ns
t <sub>SCLL</sub>	SCL Low Time	13.2		ns
t <sub>SCLH</sub>	SCL High Time	13.2		ns
t <sub>R</sub>	SCL, SDA, SEN Rise Time		6.5	ns
t <sub>F</sub>	SCL, SDA, SEN Fall Time		6.5	ns
t <sub>ESU</sub>	SEN rising edge to SCL rising edge	19.2		ns
t <sub>EHD</sub>	SCL rising edge to SEN falling edge	19.2		ns
t <sub>DSU</sub>	SDA valid to SCL rising edge	13.2		ns
t <sub>DHD</sub>	SDA valid after SCL rising edge	13.2		ns
t <sub>EOW</sub>	SEN falling edge to SEN rising edge	38.4		ns

Figure 11. Recommended Bus Sharing

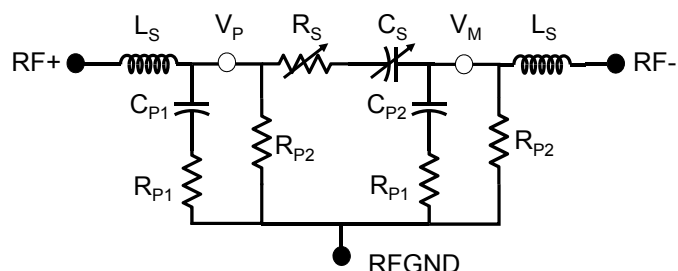


### Equivalent Circuit Model Description

The DTC Equivalent Circuit Model includes all parasitic elements and is accurate in both Series and Shunt configurations, reflecting physical circuit behavior accurately and providing very close correlation to measured data. It can easily be used in circuit simulation programs.

For  $V_P$  and  $V_M$  max operating limits, refer to *Table 3*.

**Figure 12. Equivalent Circuit Model Schematic**



**Table 7. Equivalent Circuit Model Parameters**

Variable	Equation (state = 0, 1, 2...31)	Unit
$C_S$	$0.185 \cdot \text{state} + 1.6$	pF
$R_S$	$20 / (\text{state} + 20 / (\text{state} + 0.7)) + 0.7$	$\Omega$
$R_{P1}$	$8 + 0.5 \cdot \text{state}$	$\Omega$
$R_{P2}$	$25000 + 3 \cdot \text{state}^3$	$\Omega$
$C_{P1}$	$-0.0061 \cdot \text{state} + 0.55$	pF
$C_{P2}$	$0.0096 \cdot \text{state} + 0.61$	pF
$L_S$	0.35	nH

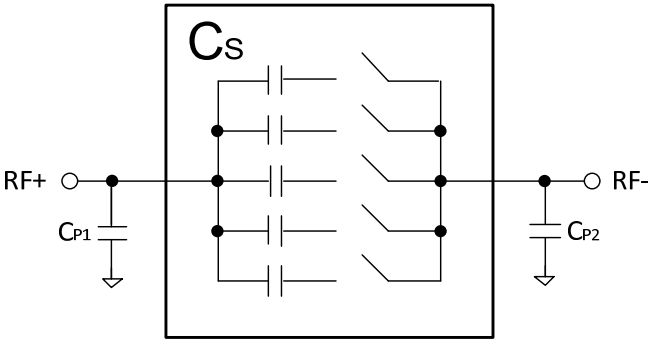
**Table 8. Equivalent Circuit Data**

State			Effective Capacitance		Equivalent Circuit Model Parameters			
Hex	Bin	Dec	Series [pF]	Shunt [pF]	$C_S$ [pF]	$R_S$ [ $\Omega$ ]	$C_{P1}$ [pF]	$C_{P2}$ [pF]
0x00	00000	0	1.60	2.15	1.60	1.40	0.55	0.61
0x01	00001	1	1.79	2.33	1.79	2.27	0.54	0.62
0x02	00010	2	1.97	2.51	1.97	2.83	0.54	0.63
0x03	00011	3	2.16	2.69	2.16	3.08	0.53	0.64
0x04	00100	4	2.34	2.87	2.34	3.12	0.53	0.65
0x05	00101	5	2.53	3.05	2.53	3.05	0.52	0.66
0x06	00110	6	2.71	3.22	2.71	2.93	0.51	0.67
0x07	00111	7	2.90	3.41	2.90	2.78	0.51	0.68
0x08	01000	8	3.08	3.58	3.08	2.64	0.50	0.69
0x09	01001	9	3.27	3.77	3.27	2.51	0.50	0.70
0x0A	01010	10	3.45	3.94	3.45	2.39	0.49	0.71
0x0B	01011	11	3.64	4.12	3.64	2.27	0.48	0.72
0x0C	01100	12	3.82	4.30	3.82	2.17	0.48	0.73
0x0D	01101	13	4.01	4.48	4.01	2.08	0.47	0.73
0x0E	01110	14	4.19	4.65	4.19	2.00	0.46	0.74
0x0F	01111	15	4.38	4.84	4.38	1.93	0.46	0.75
0x10	10000	16	4.56	5.01	4.56	1.86	0.45	0.76
0x11	10001	17	4.75	5.20	4.75	1.80	0.45	0.77
0x12	10010	18	4.93	5.37	4.93	1.75	0.44	0.78
0x13	10011	19	5.12	5.55	5.12	1.70	0.43	0.79
0x14	10100	20	5.30	5.73	5.30	1.65	0.43	0.80
0x15	10101	21	5.49	5.91	5.49	1.61	0.42	0.81
0x16	10110	22	5.67	6.09	5.67	1.57	0.42	0.82
0x17	10111	23	5.86	6.27	5.86	1.54	0.41	0.83
0x18	11000	24	6.04	6.44	6.04	1.51	0.40	0.84
0x19	11001	25	6.23	6.63	6.23	1.48	0.40	0.85
0x1A	11010	26	6.41	6.80	6.41	1.45	0.39	0.86
0x1B	11011	27	6.60	6.99	6.60	1.42	0.39	0.87
0x1C	11100	28	6.78	7.16	6.78	1.40	0.38	0.88
0x1D	11101	29	6.97	7.34	6.97	1.37	0.37	0.89
0x1E	11110	30	7.15	7.52	7.15	1.35	0.37	0.90
0x1F	11111	31	7.34	7.70	7.34	1.33	0.36	0.91

**Series Operation**

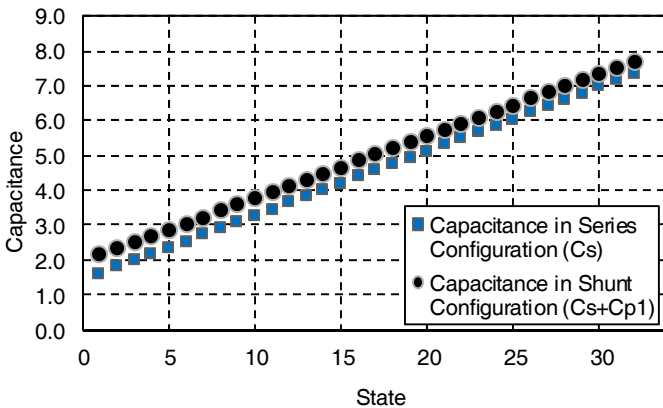
In Series configuration, the effective capacitance between RF+ and RF- ports is represented by  $C_s$  and tuning ratio as  $C_{Smax}/C_{Smin}$ .

**Figure 13. Effective Capacitance Diagram**



Shunt Configuration (looking into RF+ when RF- is grounded) will have higher total capacitance at RF+ due to parallel combination of  $C_s$  with parasitic capacitance  $C_{P1}$  ( $C_s + C_{P1}$ ), as demonstrated in Figure 14 and Table 9.

**Figure 14. Typical Capacitance vs. State**

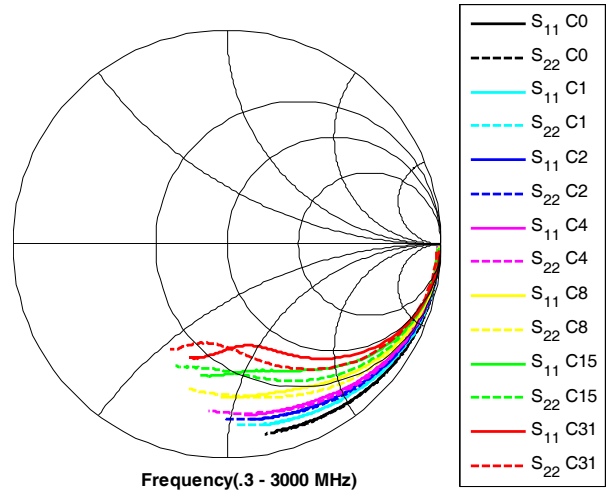


**Table 9. Effective Capacitance Summary**

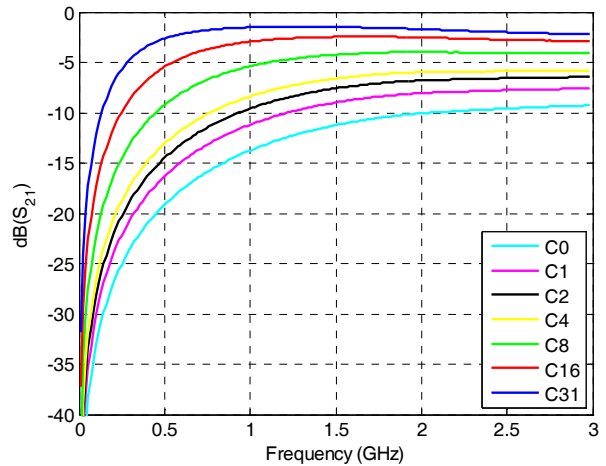
Configuration	Effective Capacitance	$C_{min}$ (state 0)	$C_{max}$ (state 31)	Tuning Ratio
Series (RF+ to RF-)	$C_s$	1.60	7.34	4.59:1
Shunt (RF+ to GND)	$C_s + C_{P1}$	2.15	7.7	3.6:1

$S_{11}$  and  $S_{21}$  for series configuration is illustrated in Figures 18 and 19.  $S_{21}$  includes mismatch and dissipative losses and is not indicative of tuning network loss. Equivalent Circuit Model can be used for simulation of tuning network loss.

**Figure 15. Measured Series  $S_{11}/S_{22}$  (major states)**



**Figure 16. Measured Series  $S_{21}$  vs. Frequency (major states)**



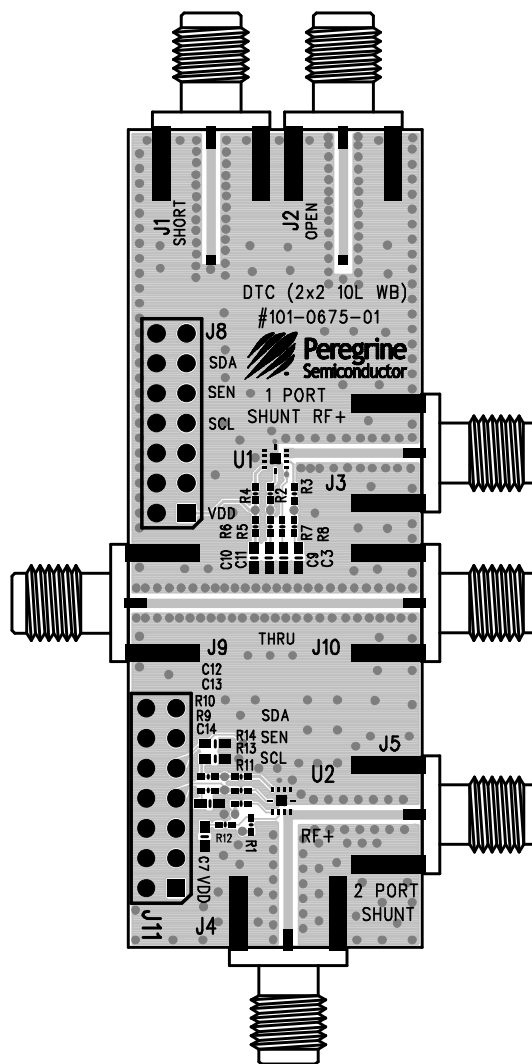
When the DTC is used as a part of a reactive network, impedance transformation may cause the internal RF voltages ( $V_P$  and  $V_M$  in Figure 12) to exceed peak operating RF voltage. The complete RF circuit must be simulated using actual input power and load conditions to ensure neither  $V_P$  nor  $V_M$  exceeds 30 Vpk.

### Evaluation Board

The 101-0675 Evaluation Board (EVB) was designed for accurate measurement of the DTC impedance and loss. Two configurations are available: 1 Port Shunt (J3) and 2 Port Shunt (J4, J5). Three calibration standards are provided. The open (J2) and short (J1) standards (104 ps delay) are used for performing port extensions and accounting for electrical length and transmission line loss. The Thru (J9, J10) standard can be used to estimate PCB transmission line losses for scalar de-embedding of the 2 Port Series configuration (J4, J5).

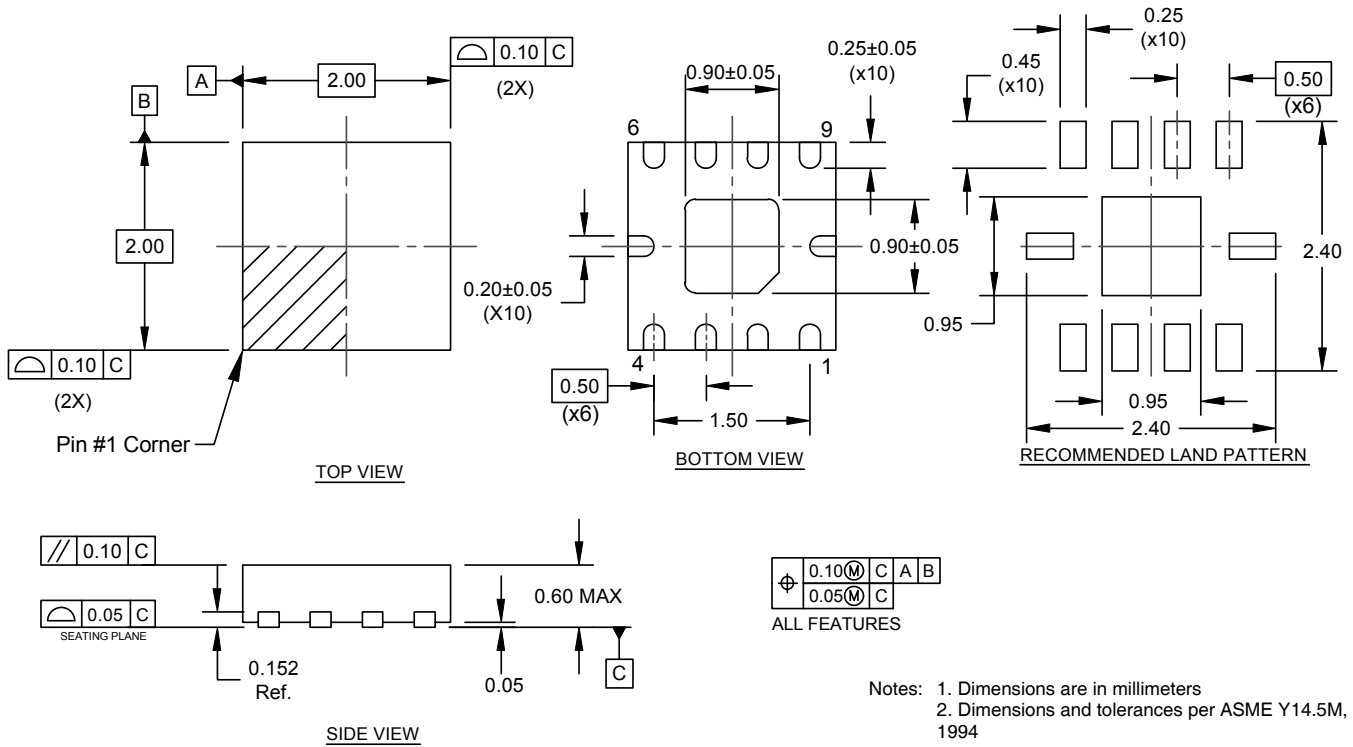
The board consists of a 4 layer stack with 2 outer layers made of Rogers 4350B ( $\epsilon_r = 3.48$ ) and 2 inner layers of FR4 ( $\epsilon_r = 4.80$ ). The total thickness of this board is 62 mils (1.57 mm). The inner layers provide a ground plane for the transmission lines. Each transmission line is designed using a coplanar waveguide with ground plane (CPWG) model using a trace width of 32 mils (0.813 mm), gap of 15 mils (0.381 mm), and a metal thickness of 1.4 mils (0.051 mm).

Figure 17. Evaluation Board

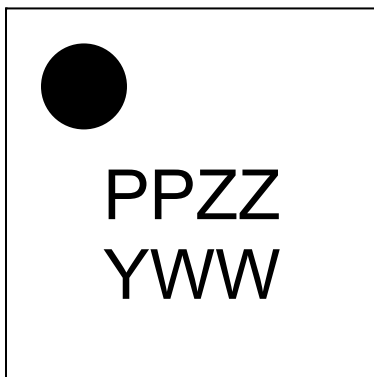




**Figure 18. Package Drawing**  
10-lead 2 x 2 x 0.55 mm



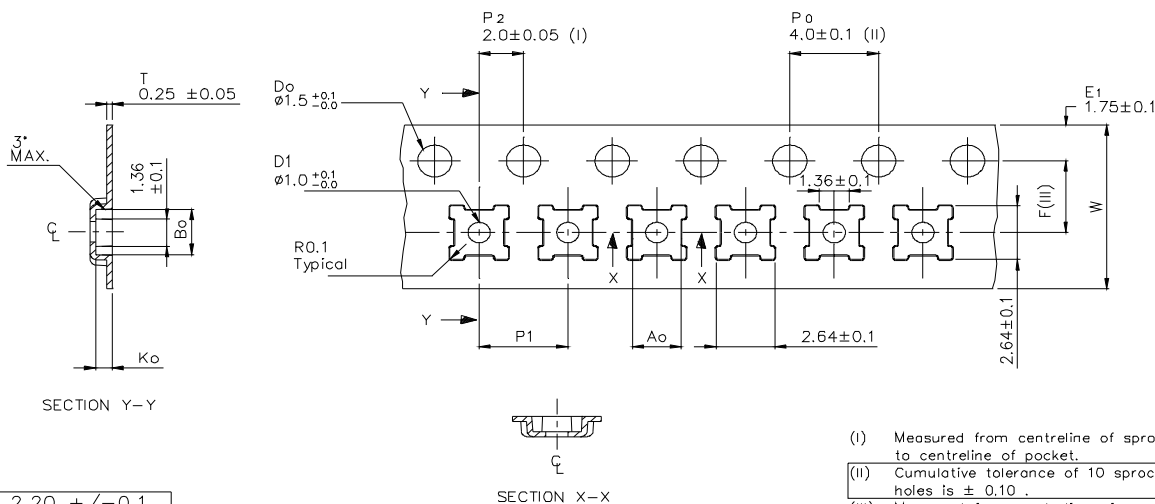
**Figure 19. Marking Specifications**



Marking Spec Symbol	Package Marking	Definition
PP	DC*	Part number marking for PE623080
ZZ	00-99	Last two digits of lot code
Y	0-9	Last digit of year, starting from 2009 (0 for 2010, 1 for 2011, etc)
WW	01-53	Work week

Note: (PP), the package marking specific to the PE623080, is shown in the figure instead of the standard Peregrine package marking symbol (P)

**Figure 20. Tape and Reel Specifications**  
10-lead 2 x 2 x 0.55 mm

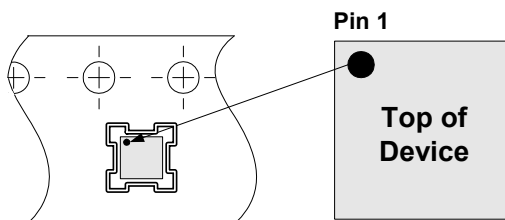


- (I) Measured from centreline of sprocket hole to centreline of pocket.
- (II) Cumulative tolerance of 10 sprocket holes is  $\pm 0.10$ .
- (III) Measured from centreline of sprocket hole to centreline of pocket.
- (IV) Other material available.

This part shall not contain any banned substance as Sony standard SS-00259

ALL DIMENSIONS IN MILLIMETRES UNLESS OTHERWISE STATED.

-----> Tape Feed Direction ----->



Device Orientation in Tape

**Table 10. Ordering Information**

Order Code	Package	Description	Shipping Method
PE623080MLAA-Z	10-lead QFN 2 x 2 x 0.55 mm	Package Part in Tape and Reel	3,000 units / T&R
EK623080-11	Evaluation Kit	Evaluation Kit	1 set / box

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For sales and contact information please visit [www.psemi.com](http://www.psemi.com).

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**Product Specification:** The datasheet contains final data. In the event Peregrine decides to change the specifications, Peregrine will notify customers of the intended changes by issuing a CNF (Customer Notification Form).  
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