Peregrine Semiconductor

Product Specification

PE42671

SP7T UltraCMOS™ 2.75 V Switch
100 – 3000 MHz, +68 dBm IIP3

Features

- 2 TX, 2 TRX, 3 RX ports
- Three pin CMOS logic control with integral decoder/driver
- Exceptional harmonic performance: $2f_o$ = -83 dBc and $3f_o$ = -77.5 dBc
- Low TX insertion loss: 0.65 dB at 900 MHz, 0.75 dB at 1900 MHz
- TX – RX Isolation of 46 dB at 900 MHz, 38 dB at 1900 MHz
- 1000 V HBM ESD tolerance all ports
- +68 dBm IIP3 @ 50 Ω
- -111 dBm IMD3
- No blocking capacitors required

Product Description

The PE42671 is a HaRP™-enhanced SP7T RF Switch developed on the UltraCMOS™ process technology. It addresses the specific design needs of the Quad-Band GSM Handset Antenna Switch Module Market for use in GSM/PCS/EDGE/WCDMA handsets. The switch is comprised of two transmit ports that can be used for GSM/PCS/EDGE, two transmit/receive ports (TRX1 and TRX2) that can be used for either WCDMA or as receive ports, and three symmetric receive ports. On-chip CMOS decode logic facilitates three-pin low voltage CMOS control, while high ESD tolerance of 1000 V at all ports, no blocking capacitor requirements, and on-chip SAW filter over-voltage protection devices make this the ultimate in integration and ruggedness.

Peregrine's HaRP™ technology enhancements deliver high linearity and exceptional harmonics performance. It is an innovative feature of the UltraCMOS™ process, providing performance superior to GaAs with the economy and integration of conventional CMOS.

Figure 1. Functional Diagram

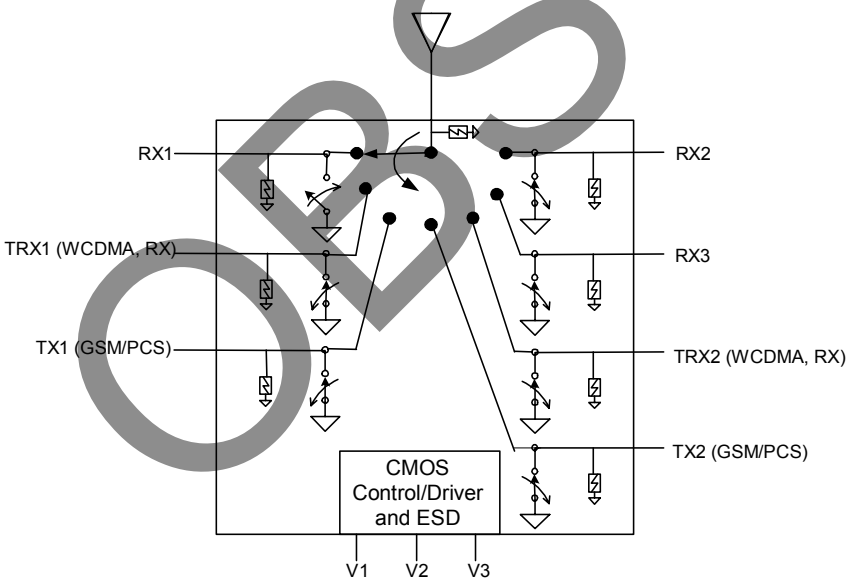


Figure 2. Die Top View

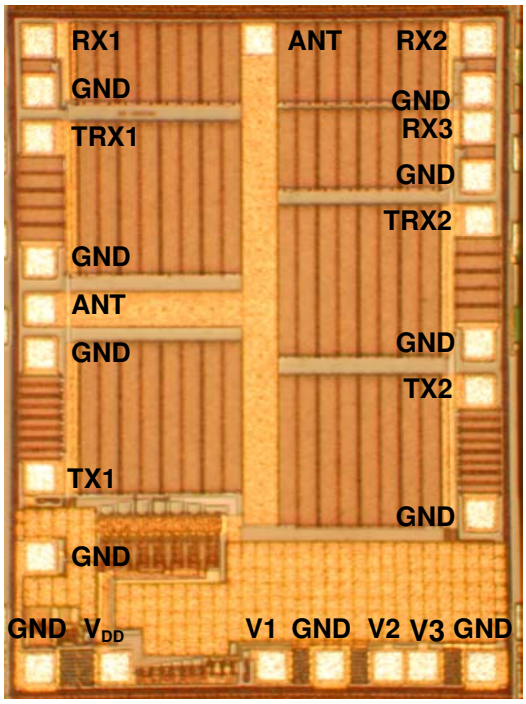


Table 1. Target Electrical Specifications @ 25 °C, V_{DD} = 2.75 V

Parameter	Condition	Min	Typ	Max	Units
Insertion loss[1]	TX - ANT (850 / 900)		0.65	0.75	dB
	TX - ANT (1800 / 1900)		0.75	0.85	dB
	TRX - ANT (850 WCDMA)		0.6	0.7	dB
	TRX - ANT (2100 WCDMA)		0.75	0.85	dB
	RX - ANT (850 / 900)		0.95	1.05	dB
	RX - ANT (1800 / 1900)		1.0	1.10	dB
Return Loss	Port under test in on state (850 / 900)	17	20		dB
	(1800 / 1900 / 2100)	12	15		dB
Isolation	TX - RX (850 / 900)	43	46		dB
	TX - RX (1800 / 1900)	35	38		dB
	TX - TX (850 / 900)	31	33		dB
	TX - TX (1800 / 1900)	23	26		dB
	TX - TRX (850 / 900)	33	36		dB
	TX - TRX (1800 / 1900)	26	29		dB
	TRX - RX (850 WCDMA)	36	39		dB
	TRX - RX (2100 WCDMA)	28	31		dB
2nd Harmonic	TX 850 / 900 MHz, +35 dBm output power, 50 Ω		-83	-78	dBc
	TX 1800 / 1900 MHz, +33 dBm output power, 50 Ω		-82	-76	dBc
3rd Harmonic	TX 850 / 900 MHz, +35 dBm output power, 50 Ω		-77.5	-72.5	dBc
	TX 1800 / 1900 MHz, +33 dBm output power, 50 Ω		-78	-73	dBc
WCDMA 2100 IMD3	TRX1 / TRX2: Measured at 2.14 GHz at ANT port, input +20 dBm CW signal at 1.95 GHz and -15 dBm CW signal at 1.76 GHz		-111	-103	dBm
WCDMA 2100 IIP3	TRX1 / TRX2: Measured at 2.14 GHz at ANT port, input +20 dBm CW signal at 1.95 GHz and -15 dBm CW signal at 1.76 GHz		+68	+64	dBm

Note: 1. Insertion loss specified with optimal impedance matching.

Table 2. Operating Ranges

Parameter	Symbol	Min	Typ	Max	Units
Temperature range	T_{OP}	-40		+85	°C
V_{DD} Supply Voltage	V_{DD}	2.65	2.75	2.85	V
I_{DD} Power Supply Current (V_{DD} = 2.75 V)	I_{DD}		13	50	µA
TX input power[2] (VSWR ≤ 3:1) 824-915 MHz	P_{IN}			+35	dBm
TX input power[2] (VSWR ≤ 3:1) 1710-1910 MHz				+33	
TRX input power (VSWR ≤ 3:1) 824 - 2170 MHz				+31	
RX input power[2] (VSWR =1:1)	P_{IN}			+20	dBm
Control Voltage High	V_{IH}	1.4			V
Control Voltage Low	V_{IL}			0.4	V

Note: 2. Assumes RF input period of 4620 µs and duty cycle of 50%.

Figure 3. Pad Configuration (Top View)

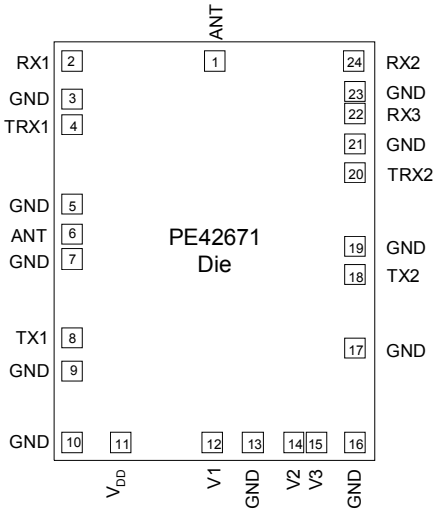


Table 4. Pin Descriptions

Pin No.	Pin Name	Description
1	ANT	RF Common – Antenna Redundant ANT pins for flexible bonding
2	RX1[4]	RF I/O – RX1
3	GND[3]	Ground
4	TRX1[4]	RF I/O – TRX1
5	GND[3]	Ground
6	ANT	RF Common – Antenna Redundant ANT pins for flexible bonding
7	GND[3]	Ground
8	TX1[4]	RF I/O - TX1
9	GND[3]	Ground
10	GND[3]	Ground
11	V_{DD}	Supply
12	V1	Switch control input, CMOS logic level
13	GND[3]	Ground
14	V2	Switch control input, CMOS logic level
15	V3	Switch control input, CMOS logic level
16	GND[3]	Ground
17	GND[3]	Ground
18	TX2[4]	RF I/O – TX2
19	GND[3]	Ground
20	TRX2[4]	RF I/O – TRX2
21	GND[3]	Ground
22	RX3[4]	RF I/O – RX3
23	GND[3]	Ground
24	RX2[4]	RF I/O – RX2

Notes: 3. Bond wires should be physically short and connected to ground plane for best performance.
4. Blocking capacitors needed only when non-zero DC voltage present.

Table 3. Absolute Maximum Ratings

Symbol	Parameter/Conditions	Min	Max	Units
V_{DD}	Power supply voltage	-0.3	4.0	V
V_I	Voltage on any DC input	-0.3	V_{DD}+ 0.3	V
T_{ST}	Storage temperature range	-65	+150	°C
P_{IN} (50 Ω)	TX input power (50 Ω)[5,6] 824-915 MHz		+38	dBm
	TX input power (50 Ω)[5,6] 1710-1910 MHz		+36	
	TRX input power (50 Ω) 824 - 2170 MHz		+34	
	RX input power (50 Ω)[5,6]		+23	
P_{IN} (∞:1)	TX input power (VSWR = (∞:1)[5,6] 824-915 MHz		+35	dBm
	TX input power (VSWR = (∞:1)[5,6] 1710-1910 MHz		+33	
	TRX input power (VSWR = (∞:1) 824 - 2170 MHz		+31	
V_{ESD}	ESD Voltage (HBM, MIL_STD 883 Method 3015.7)		1000	V

Note: 5. Assumes RF input period of 4620 µs and duty cycle of 50%.
6. V_{DD} within operating range specified in Table 2.

Part performance is not guaranteed under these conditions. Exposure to absolute maximum conditions for extended periods of time may adversely affect reliability. Stresses in excess of absolute maximum ratings may cause permanent damage.

Table 5. Truth Table

Path	V3	V2	V1
TX1 - ANT	0	0	0
TX2 - ANT	0	0	1
TRX1 - ANT	0	1	0
TRX2 - ANT	1	1	0
RX1 - ANT	0	1	1
RX2 - ANT	1	0	0
RX3 - ANT	1	0	1

Electrostatic Discharge (ESD) Precautions

When handling this UltraCMOS™ device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the specified rating.

Latch-Up Avoidance

Unlike conventional CMOS devices, UltraCMOS™ devices are immune to latch-up.

Evaluation Kit

The SP7T Evaluation Kit board was designed to ease customer evaluation of the PE42671 RF switch.

The PE42671 has two high power transmit (TX) ports, two transmit/receive (TRX) ports, and three high isolation RX ports. The TX ports are designed as paths for GSM 850, 900, 1800, or 1900 MHz bands, while the TRX ports are designed for WCDMA or as transmit/receive ports. The RX ports are symmetric and can be assigned to any of the GSM frequency bands.

The ANT port connects through a 50 Ω transmission line to the bottom left SMA connector, J3. The RX, TX, and TRX ports connect through 50 Ω transmission lines to SMA connectors J1, J2 and J4 – J8.

J12 supplies DC power to the pin marked V_{DD} and the bottom row of pins, which is GND. 1 MΩ pull-up resistors are connected from V_{DD} to each of the three control logic inputs: V1, V2, and V3. These pull-up resistors are provided for ease of evaluation on this board and are not required for the PE42671 to operate.

Adding a jumper between a control pin and the adjacent GND pin on the bottom row of J12 will set a logic-0 on that control pin. Removing the jumper will set a logic-1. To evaluate the PE42671, add or remove jumpers according to the truth table in Table 5.

Figure 4. Evaluation Board Layout
Peregrine Specification 101/0261

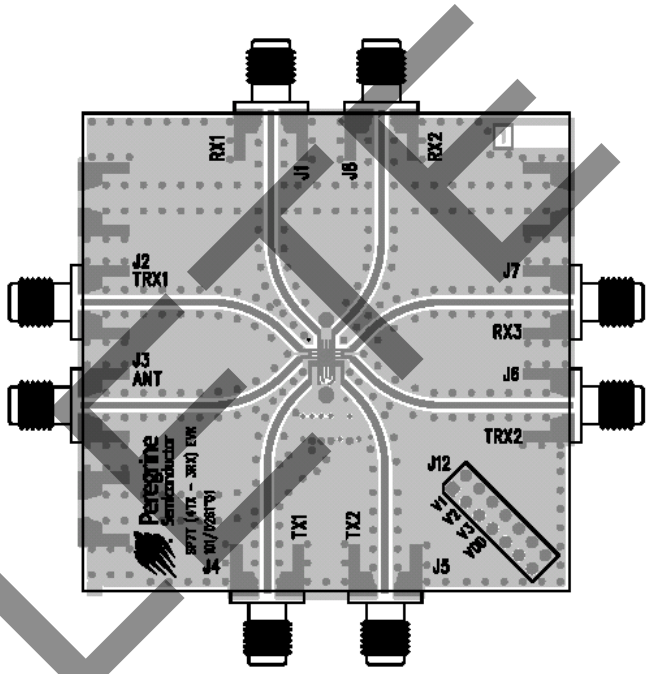
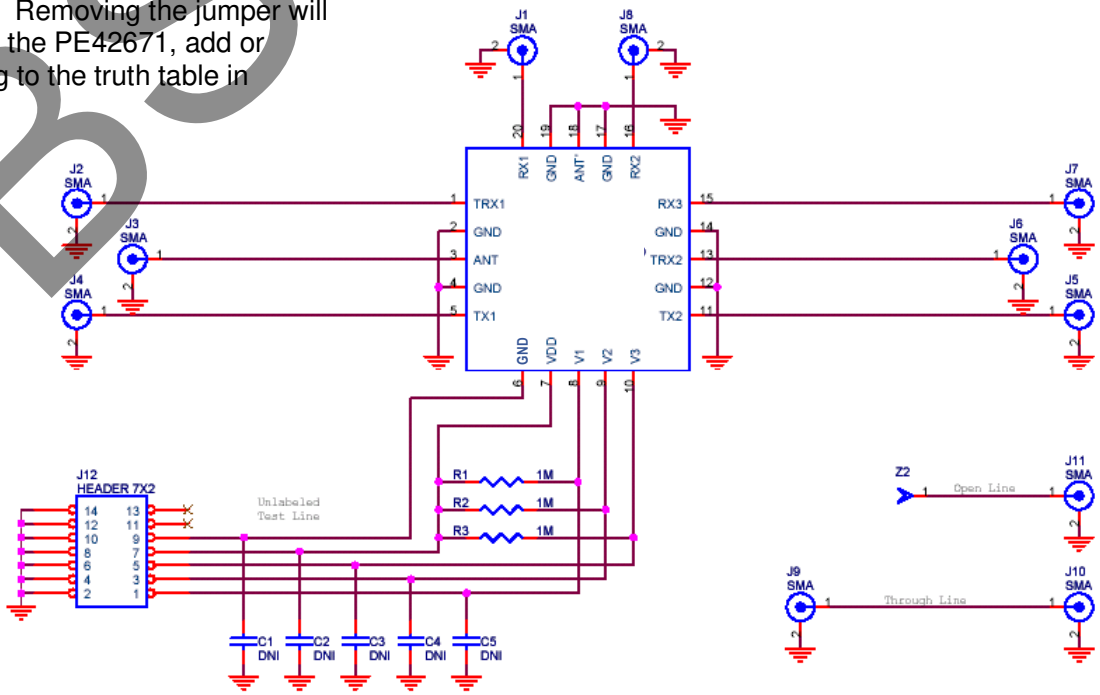


Figure 5. Evaluation Board Schematic
Peregrine Specification 102/0328



Typical Performance Data

Figure 6. Insertion Loss: RX @ 25 °C

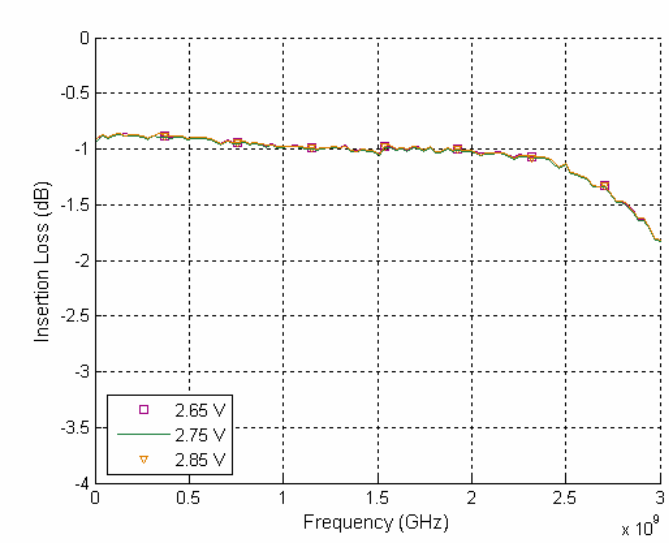


Figure 7. Insertion Loss: RX @ 2.75 V

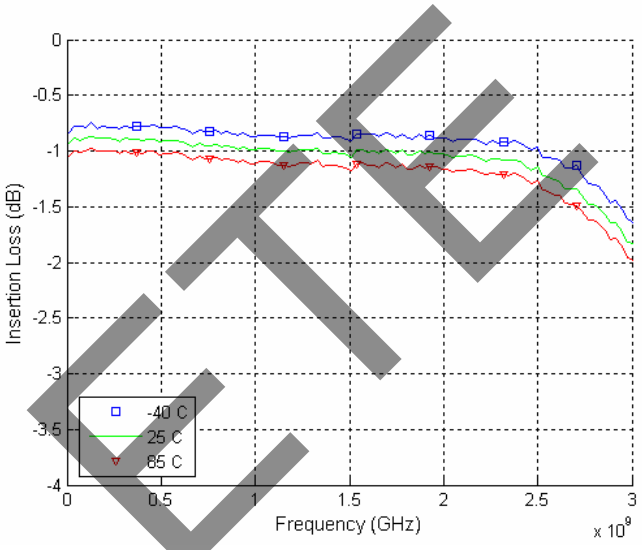


Figure 8. Insertion Loss: TRX @ 25 °C

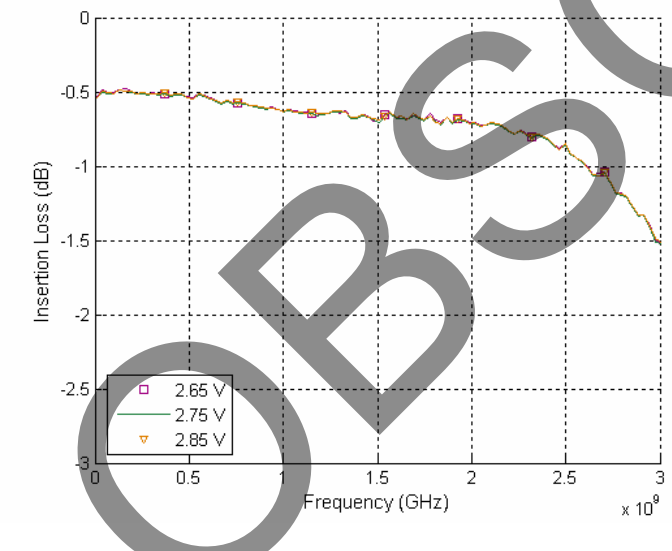
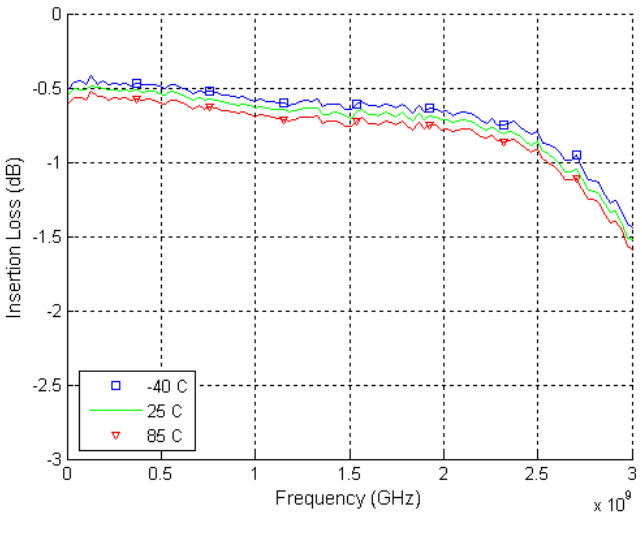


Figure 9. Insertion Loss: TRX @ 2.75 V



Note: Graphs shown with optimal impedance matching.

Typical Performance Data

Figure 10. Insertion Loss: TX @ 25 °C

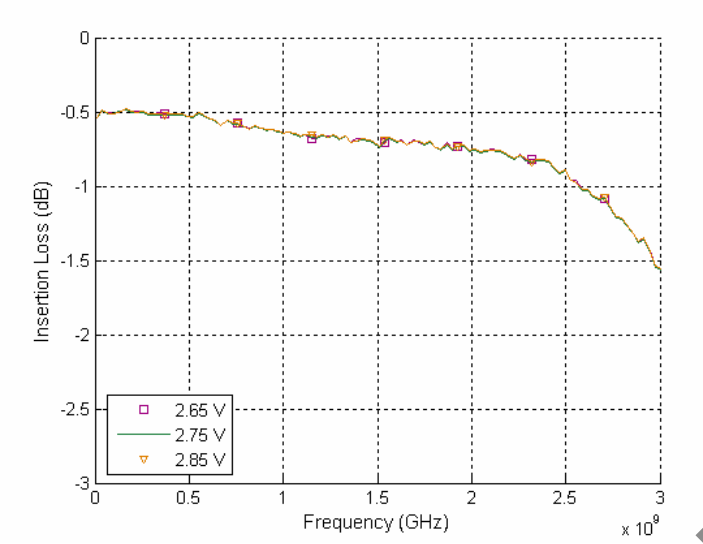


Figure 11. Insertion Loss: TX @ 2.75 V

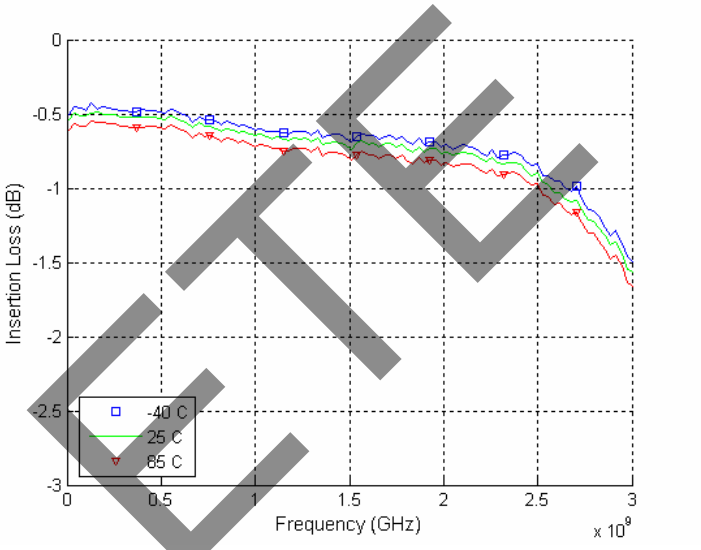


Figure 12. Isolation: TX to RX @ 25 °C

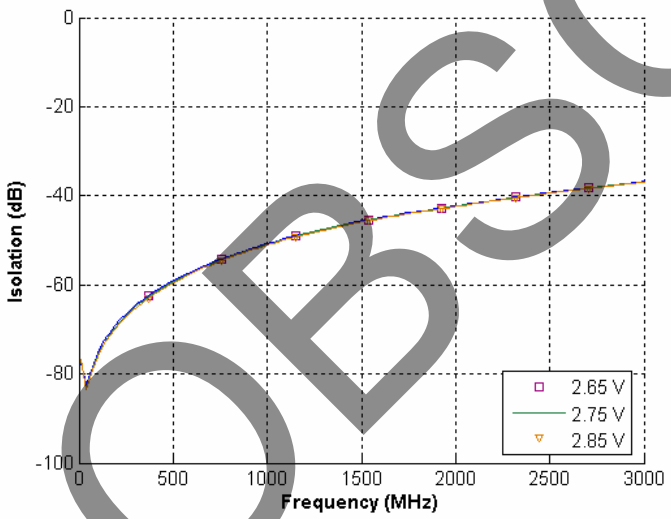
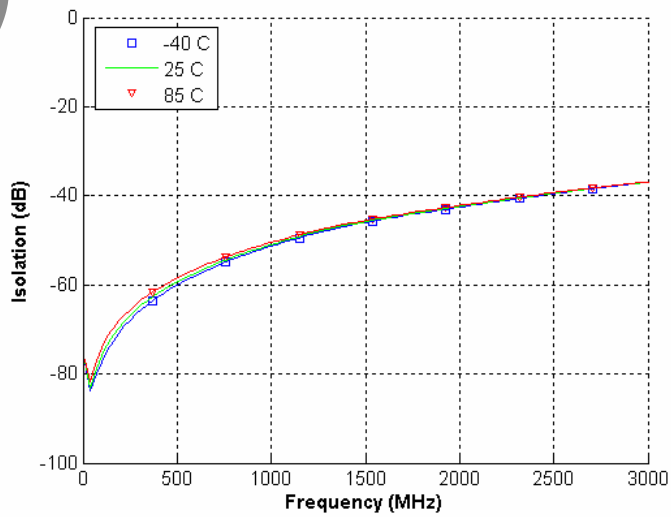


Figure 13. Isolation: TX to RX @ 2.75 V



Note: Graphs shown with optimal impedance matching.

Typical Performance Data

Figure 14. Isolation: TX to TRX @ 25 °C

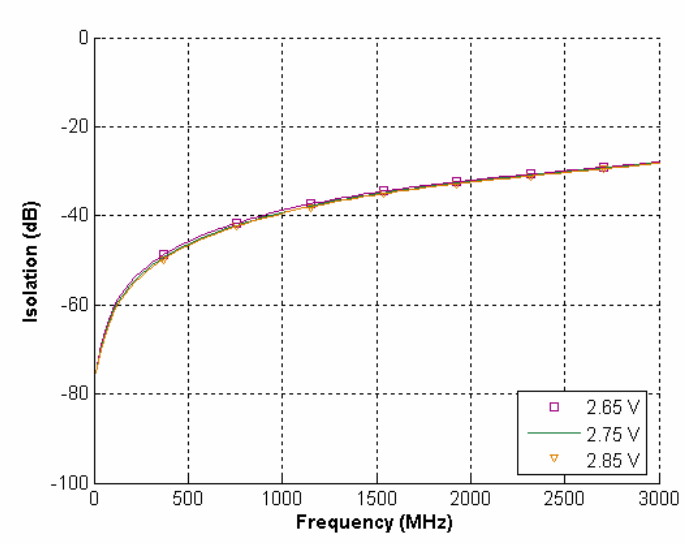


Figure 15. Isolation: TX to TRX @ 2.75 V

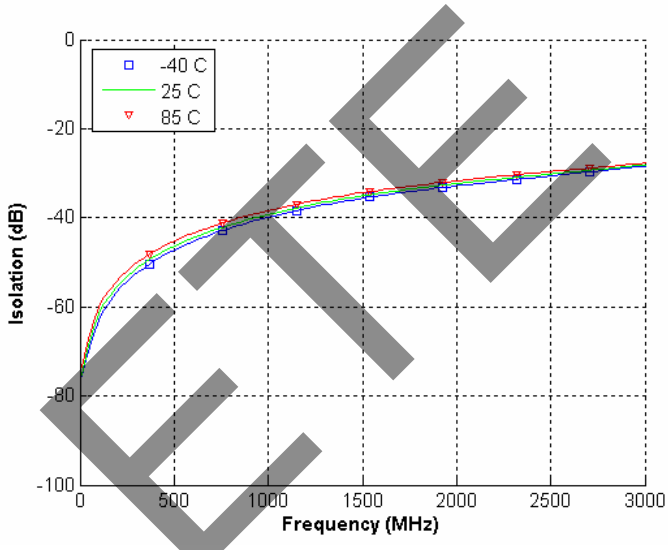


Figure 16. Isolation: TX to TX @ 25 °C

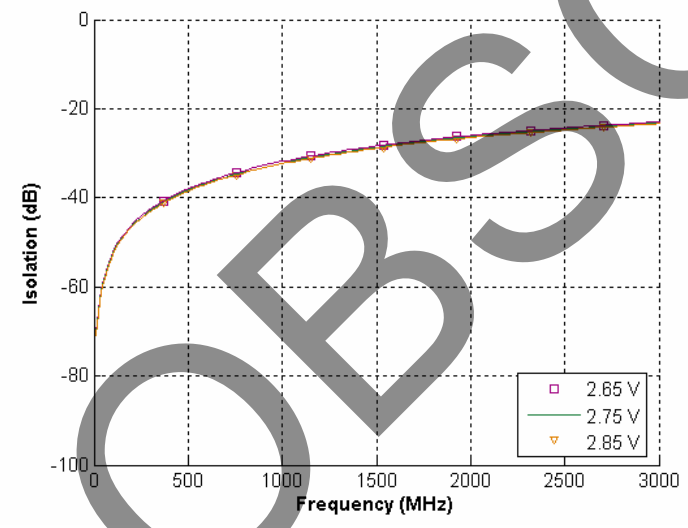
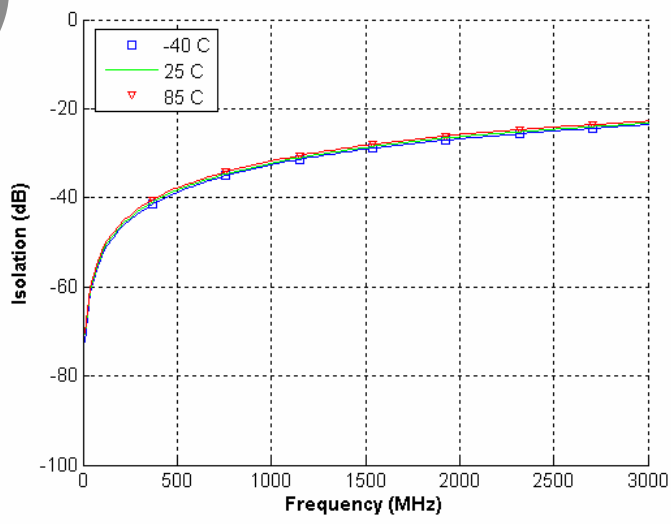


Figure 17. Isolation: TX to TX @ 2.75 V



Note: Graphs shown with optimal impedance matching.

Typical Performance Data

Figure 18. Isolation: TRX to RX @ 25 °C

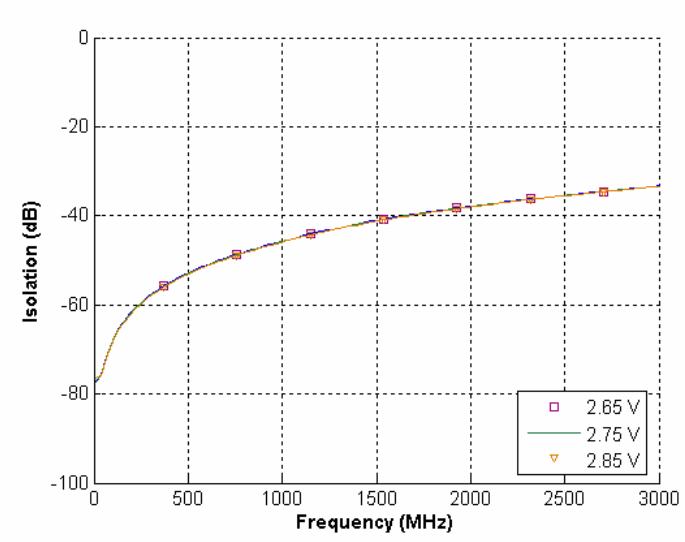


Figure 19. Isolation: TRX to RX @ 2.75 V

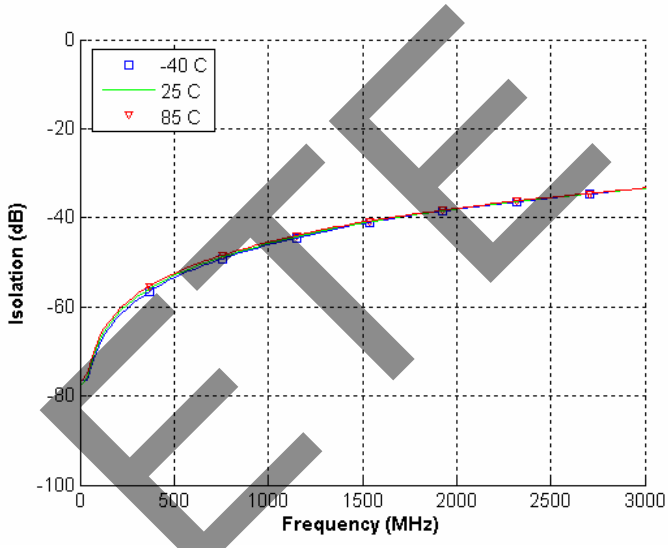


Figure 20. Return Loss: RX @ 25 °C

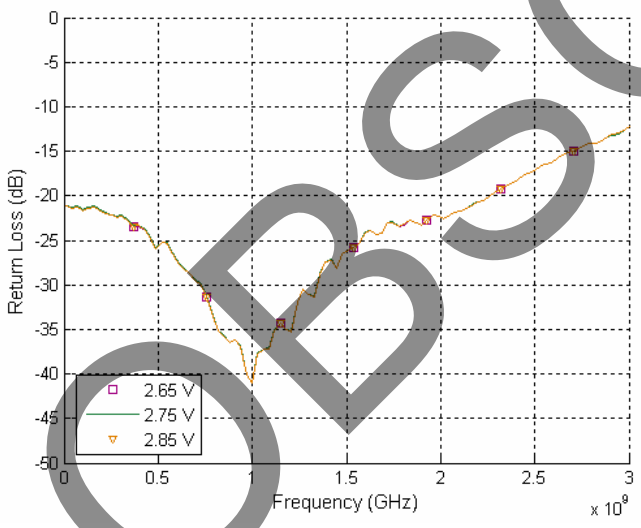
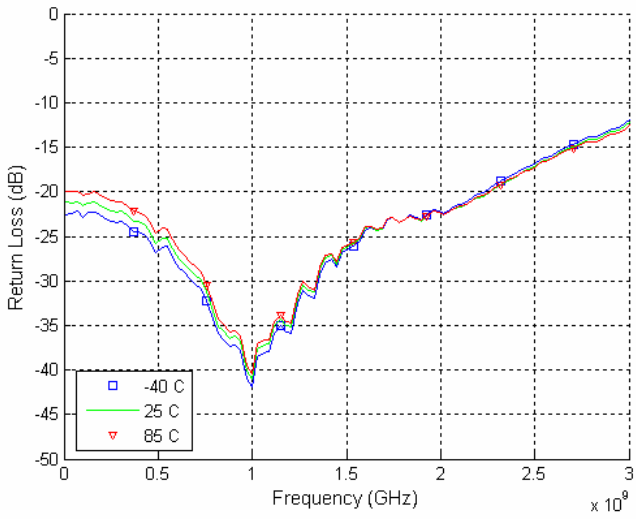


Figure 21. Return Loss: RX @ 2.75 V



Note: Graphs shown with optimal impedance matching.

Typical Performance Data

Figure 22. Return Loss: TRX @ 25 °C

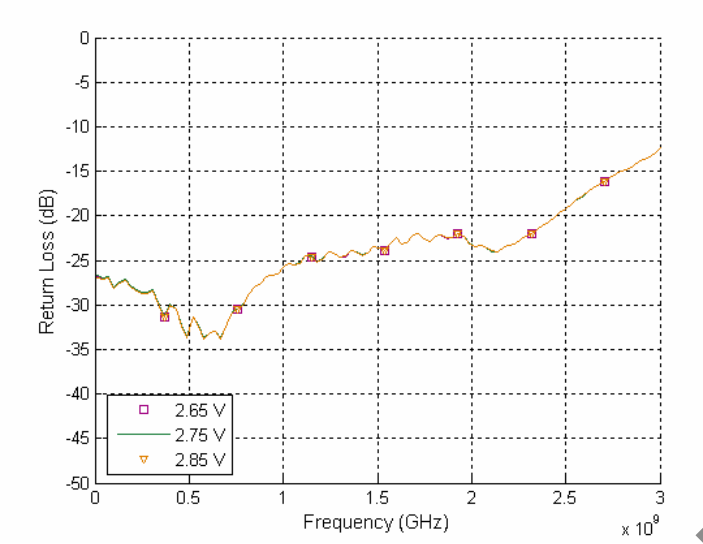


Figure 23. Return Loss: TRX @ 2.75 V

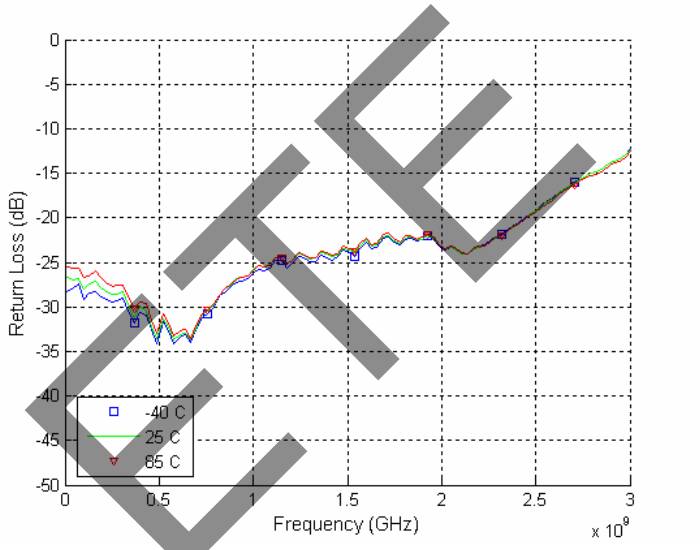


Figure 24. Return Loss: TX @ 25 °C

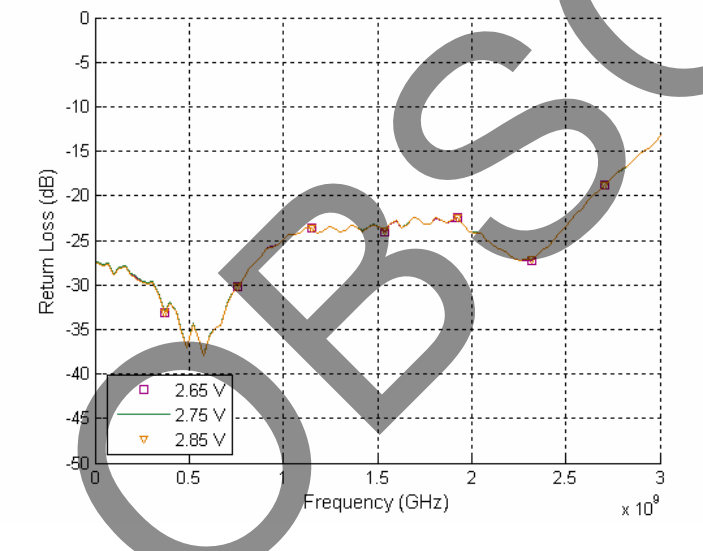
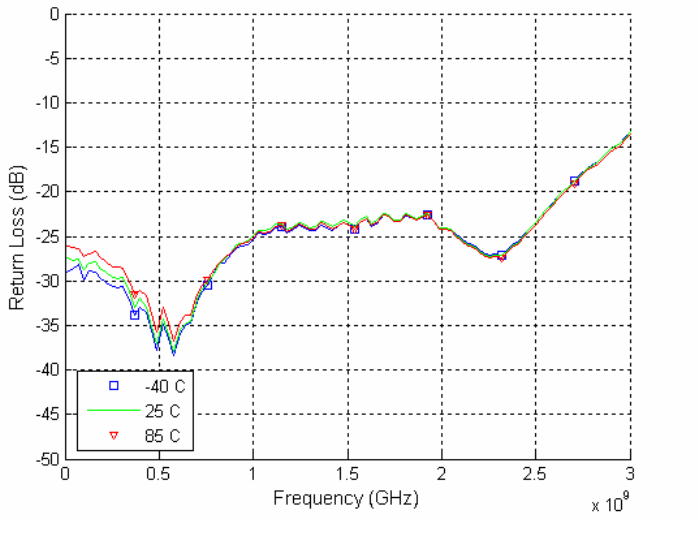


Figure 25. Return Loss: TX @ 2.75 V



Note: Graphs shown with optimal impedance matching.

Electrical Test and Performance Specifications

PE42671 dice are 100% electrically tested for the parameters listed below from Table 1 and Table 2. All other parameters are guaranteed through design and characterization.

- Insertion Loss (all ports)
- TX1, TX2 and TRX1, TRX2 Harmonics
- TX – RX Isolation
- TRX – RX Isolation
- I_{DD} supply current
- Control pin leakages

Wafer and Die Packaging

Peregrine Semiconductor has two methods for shipping dice to our customers. The shipping option used is based on the customer's requirements and the number of dice.

Peregrine offers product dice in two packaging options: Standard Die Carrier Packages (waffle pack) and dice on Film Frames.

Wafer Mount/Dicing

In preparation for dicing, wafers are thinned and polished and 100% electrically probed prior to mounting on film frame tape and rings. Figure 26 shows a wafer mounted on film frame using PVC backed mounting tape. In preparation for shipment, wafers are visually inspected after singulation and shipped with an electronic map file providing good dice locations.

Storage and Preservation

Proper storage conditions are necessary to prevent product contamination and/or degradation after shipment.

Product should be stored in the original unopened packaging or, once opened, in a nitrogen purged cabinet at room temperature (45% + 15% relative humidity controlled environment).

Singulated wafers mounted on film frames are intended for immediate use and have a limited shelf life. This is primarily due to the nature of the adhesive tape used for mounting the product. This product can be stored up to 6 months. This is only if the material has remained in its original sealed container. To reduce the risk of contamination or degradation, it is recommended that product not being used in the assembly process be returned to their original containers and resealed with a vacuum seal process.

Figure 26. Wafer on Film Frame

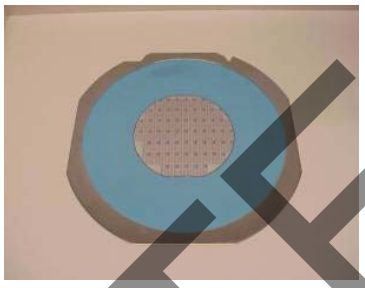


Figure 27. Dice and Wafer Processing Flow

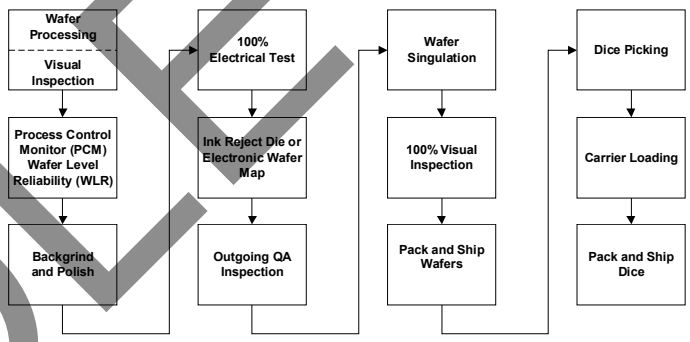
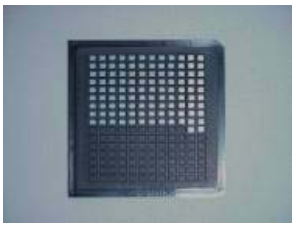


Figure 28. Waffle Pack



Standard Die Carrier Package/Waffle Pack

Waffle packs are available to customers during product development and prototyping phase only. Orders will move to film frames at production launch or for large quantity requirements.

Dice have been 100% electrically probed, singulated, visually inspected and are packaged in a 2"x2" waffle pack (304 dice per waffle pack).

Die Handling

All die products must be handled only at ESD safe workstations using standard ESD precautions. It is recommended that the die be handled only in a class 10,000 or better designated clean room environment.

Singulated dice are not to be handled with tweezers. A vacuum wand with a non-metallic ESD protected tip must be used.

Recommended Dice Assembly Procedure

Cleaning

Dice do not require cleaning prior to assembly.

Die Attach

The PE42671 die substrate is sapphire – the recommended die attach operation for sapphire is epoxy die attach adhesive. An eutectic die attach method does not work with sapphire substrates.

Bonding

Thermo compression gold ball or aluminum ultrasonic bonding may be used. The ball should cover the bonding pad, but not excessively, or it may short out the surrounding metallization. Aluminum or gold 1-mil wire is recommended. Note the bonding pad material is aluminum.

Shipping Method

Standard die carrier packages and wafer film frames are placed in a wafer container and then vacuum-sealed inside an ESD shielded bag. Sealed product is then placed inside a corrugated cardboard box surrounded by bubble wrap or foam for maximum protection during shipment.

Table 6. Mechanical Specifications

Parameter	Minimum	Typical	Maximum	Units	Test Conditions
Die Size, Drawn (x,y)		1156 x 1576		µm	As drawn
Die Size, Singulated (x,y)		1260 x 1680		µm	Including excess sapphire, max. tolerance = ±0.1mm in either dimension
Wafer Thickness	180	200	220	µm	
Wafer Size		150		mm	

Table 7. Pad Coordinates

Pad #	Pad Name	Pad Center (µm)	
		X	Y
1	ANT	-0.2	729.1
2	RX1	-510.4	723.5
3	GND	-510.4	609.7
4	TRX1	-513.9	502.9
5	GND	-513.9	214.1
6	ANT	-513.3	102
7	GND	-513.9	-2
8	TX1	-513.9	-290.8
9	GND	-512.6	-475.4
10	GND	-512.6	-728.1
11	V_{DD}	-339	-728.1
12	V1	24.4	-728.1
13	GND	159.6	-728.1
14	V2	294.8	-728.1
15	V3	374.8	-728.1
16	GND	510	-728.1
17	GND	512.9	-380
18	TX2	512.9	-91.2
19	GND	512.9	20.3
20	TRX2	512.9	309.1
21	GND	508.3	411.1
22	RX3	508.3	524.9
23	GND	508.3	609.7
24	RX2	508.3	723.5

All pad locations originate from the die center and refer to the center of the pad.

All pad openings are 60 x 60 µm.
Minimum pad pitch is 80 µm.

Figure 29. Pad Numbering

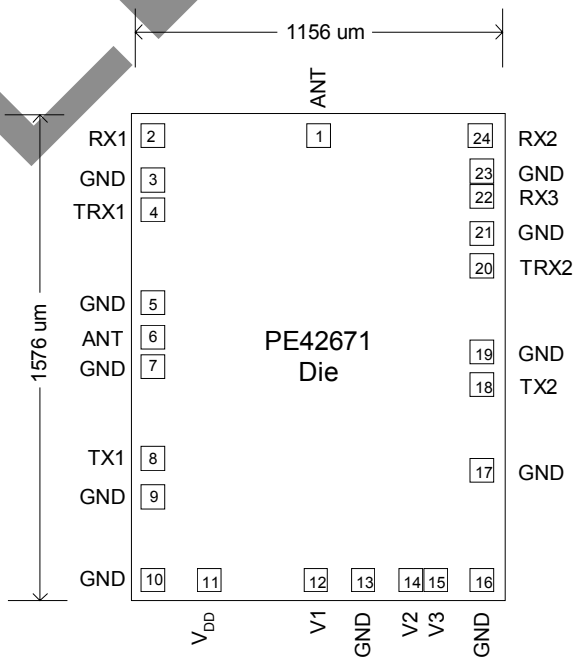


Table 8. Ordering Information

Order Code	Description	Package	Shipping Method
42671-90	PE42671-DIE-D	Film Frame	Wafer (Gross Die / Wafer Quantity)
42671-99	PE42671-DIE-304G	Waffle Pack	304 Dice / Waffle Pack
42671-00	PE42671-DIE-1H	Evaluation Kit	1/ box

Sales Offices

The Americas

Peregrine Semiconductor Corporation
9450 Carroll Park Drive
San Diego, CA 92121
Tel: 858-731-9400
Fax: 858-731-9499

Europe

Peregrine Semiconductor Europe
Bâtiment Maine
13-15 rue des Quatre Vents
F-92380 Garches, France
Tel: +33-1-4741-9173
Fax : +33-1-4741-9173

Space and Defense Products

Americas:

Tel: 858-731-9453

Europe, Asia Pacific:

180 Rue Jean de Guiramand
13852 Aix-En-Provence Cedex 3, France
Tel: +33-4-4239-3361
Fax: +33-4-4239-7227

Peregrine Semiconductor, Asia Pacific (APAC)
Shanghai, 200040, P.R. China
Tel: +86-21-5836-8276
Fax: +86-21-5836-7652

Peregrine Semiconductor, Korea
#B-2607, Kolon Tripolis, 210
Geumgok-dong, Bundang-gu, Seongnam-si
Gyeonggi-do, 463-943 South Korea
Tel: +82-31-728-3939
Fax: +82-31-728-3940

Peregrine Semiconductor K.K., Japan
Teikoku Hotel Tower 10B-6
1-1-1 Uchisaiwai-cho, Chiyoda-ku
Tokyo 100-0011 Japan
Tel: +81-3-3502-5211
Fax: +81-3-3502-5213

For a list of representatives in your area, please refer to our Web site at: ***www.psemi.com***

Data Sheet Identification

Advance Information

The product is in a formative or design stage. The data sheet contains design target specifications for product development. Specifications and features may change in any manner without notice.

Preliminary Specification

The data sheet contains preliminary data. Additional data may be added at a later date. Peregrine reserves the right to change specifications at any time without notice in order to supply the best possible product.

Product Specification

The data sheet contains final data. In the event Peregrine decides to change the specifications, Peregrine will notify customers of the intended changes by issuing a DCN (Document Change Notice).

The information in this data sheet is believed to be reliable. However, Peregrine assumes no liability for the use of this information. Use shall be entirely at the user's own risk.

No patent rights or licenses to any circuits described in this data sheet are implied or granted to any third party.

Peregrine's products are not designed or intended for use in devices or systems intended for surgical implant, or in other applications intended to support or sustain life, or in any application in which the failure of the Peregrine product could create a situation in which personal injury or death might occur. Peregrine assumes no liability for damages, including consequential or incidental damages, arising out of the use of its products in such applications.

The Peregrine name, logo, and UTSi are registered trademarks and UltraCMOS and HaRP are trademarks of Peregrine Semiconductor Corp.