

PE4120DIE

Product Description

The PE4120 is an ultra-high linearity, passive broadband Quad MOSFET array with high dynamic range. This quad array operates with differential signals at all ports (RF, LO, IF). Typical applications range from frequency up/down-conversion to phase detection for Cellular / PCS Base Stations, Wireless Broadband Communications and STB / Cable modems.

The PE4120 is manufactured in Peregrine's patented Ultra Thin Silicon (UTSi®) CMOS process, offering the performance of GaAs with the economy and integration of conventional CMOS.

Ultra-High Linearity Broadband Quad MOSFET Array

Features

- Quad MOSFET array for mixer applications
- Ultra-high linearity, broadband performance
- Up / down conversion
- Low conversion loss
- High LO Isolation

Figure 1. Functional Schematic Diagram

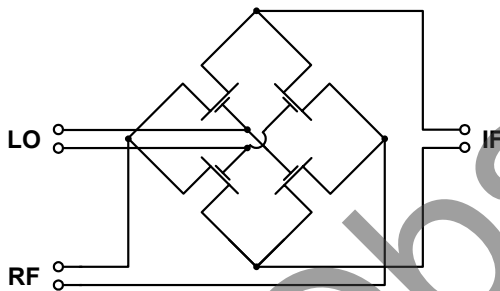


Figure 2. Die Photo

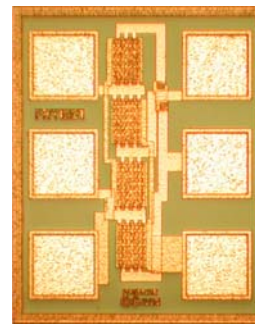
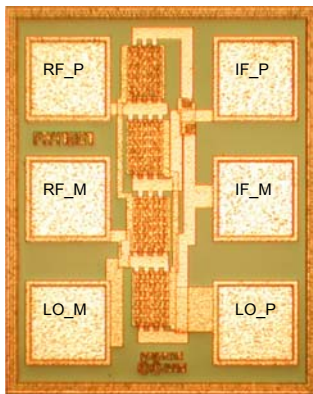


Table 1. DC Electrical Specifications @ +25 °C

Symbol	Characteristics	Min	Typ	Max	Units	Test Conditions
V_{DS}	Drain-Source Voltage	270	320	410	mV	$V_{GS} = +3V, I_{DS} = 20mA$
V_{DS} Match	Drain-Source Voltage Match		7	20	mV	$V_{ds\ max} - V_{ds\ min}$
$R_{ds\ ON}$	Drain-Source on Resistance	13.5	16	20.5	Ω	
R_{ds} Mismatch	Drain-Source Match		0.35	1	Ω	
Gate Oxide	Gate leakage			10	nA	$V_G = 5V, V_D = GND, V_S = GND$
V_T	Threshold Voltage		-100		mV	$V_{DS} = 0.1V$; per ASTM F617-00

Table 2. Mechanical Specifications

Parameter	Min	Typ	Max	Units	Test Conditions
Die Size		496x586		μm	
Chips & Cracks		1		%	100 samples / wafer
Wafer thickness	7.5	8.0	8.5	mils	
Wafer Size		150		mm	

Figure 3. Pin Configuration

Table 2. Pin Descriptions

Pad No.	Pin Name	Description
1	RF_P	RF Input Connection (Source)
2	RF_M	RF Input Connection (Source)
3	LO_M	LO Input Connection (Gate)
4	LO_P	LO Input Connection (Gate)
5	IF_M	IF Output Connection (Drain)
6	IF_P	IF Output Connection (Drain)

Table 3. Absolute Maximum Ratings

Symbol	Parameter/Conditions	Min	Max	Units
T_{ST}	Storage temperature range	-65	150	°C
T_{OP}	Operating temperature range	-40	85	°C
V_{DC+AC}	Maximum DC plus peak AC voltage across Drain-Source		±3.3	V
V_{DC+AC}	Maximum DC plus peak AC voltage across Gate-Drain or Gate-Source		±4.2	V
V_{ESD}	ESD Sensitive Device *		5	V

* The PE4120 was designed for high performance and has no ESD protection circuitry. Special care must be taken during handling.

Electrostatic Discharge (ESD) Precautions

This MOSFET device has minimally protected inputs and is highly susceptible to ESD damage. When handling this UTSi device, observe the same precautions that you would use with other ESD-sensitive devices.

Latch-Up Avoidance

Unlike conventional CMOS devices, UTSi CMOS devices are immune to latch-up.

Device Description

The PE4120 passive broadband Quad MOSFET array is designed for use in up-conversion and down-conversion applications for high performance systems such as cellular infrastructure equipment and STB/CATV systems.

The PE4120 is an ideal mixer core for a wide range of mixer products, including module level solutions that incorporate baluns or other single-ended matching structures enabling three-port operation.

The performance level of this passive mixer is made possible by the very high linearity afforded by Peregrine's UTSi CMOS process.

Wafer and Die Packaging Options

Peregrine Semiconductor has two methods for shipment of die to our customers. The shipping option used is based on the customer's requirements and the number of die being shipped.

Peregrine offers product dice in two packaging options: Standard Die Carrier Packages and Wafer Packages. Where no shipping method is specified, Peregrine will ship in Standard Die Carrier Package (waffle pack).

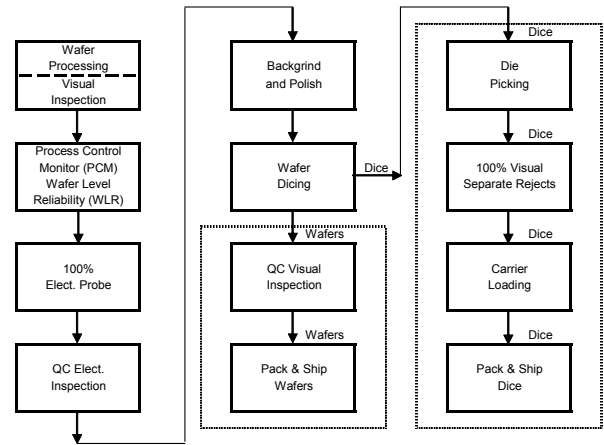
Standard Die Carrier Package

- Chips which have been electrically probed, inked, visually inspected, and diced, may be packaged in 4"x4" Waffle Packs.
- Standard die carrier packages protect the product from mechanical damage during shipment and prevent individual die from contacting one another
- The containers also provide protection from static discharge, moisture and other contamination by sealing in the proper static and moisture protective bags.
- Die are held in cavities with defined matrix. Ideal for small volumes.
- Die orientation is indicated on the label.
- 100% electrically probed dice with electrical rejects removed.
- 100% visually sorted with mechanical and visual rejects removed.
- Easy visual inspection – dice in carriers, geometry side up.
- Carrier holds 100 dice.

Figure 12. Waffle Pack



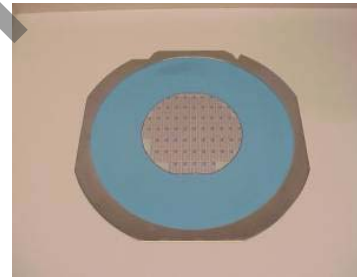
Figure 13. Dice and Wafer Processing Flow



Wafer Package

Wafers which have been electrically probed, inked, visually inspected and diced.

Figure 14. Wafer Mount



Wafer Mount/Dicing

In preparation for dicing, wafers are mounted to film frames or rings with mounting tape. There are two types of tape that can be utilized: PVC backed or U.V. release tape. Figure 14 shows a wafer mounted on a film frame using PVC backed mounting tape.

- 100% electrically probed – rejects inked
- Preferred for production quantities
- Lowest cost
- Wafer is supplied, thinned and diced

Wafer and Die Package, Storage and Preservation

Proper storage conditions are necessary to prevent product contamination and/or degradation after shipment.

- Product should be stored in original unopened packaging or, once opened, in a Nitrogen purged cabinet at room temperature (45% +/- 15% RH controlled environment).
- Sawn wafers mounted on dicing tape are intended for immediate use and have a limited shelf life. This is primarily due to the nature of the adhesive tape used for mounting the product. This product can be stored for up to 30 days. This applies whether or not the material has remained in its original sealed container. To reduce the risk of contamination or degradation, it is recommended that product not being used in the assembly process be returned to their original containers and resealed with a vacuum seal process.
- In all cases, the customer must determine the applicability of extended storage durations and conditions with respect to their assembly process and end product criteria.

Die Handling

All die products must be handled only at ESD safe workstations. Standard ESD precautions and safe work environments are as defined in MIL-HDBK-263. ESD wrist strap and cord must be worn at a static safe workstation to eliminate failures due to ESD. Product must be handled only in a class 10,000 or better designated clean room environment.

Singulated die are not to be handled with tweezers. A vacuum wand with a non-metallic ESD protected

tip should be used. Automated Wafer and Die Handling systems are readily available and provide the highest degree of protection and consistency to the handling operation.

Recommended Dice Assembly Procedure

Cleaning

Dice supplied in die or wafer form do not require cleaning prior to assembly.

Die Attach

The Peregrine Semiconductor die substrate is sapphire and the recommended die attach operation uses epoxy die attach adhesive. The eutectic die attach method does not work with sapphire substrates.

Bonding

Thermocompression gold ball or aluminum ultrasonic bonding may be used. The gold ball should be about three times the diameter of the gold wire. The ball should cover the bonding pad, but not excessively, or it may short out surrounding metallization. Aluminum 1-mil wire may be used on most dice, but should not be used if the assembled unit will be plastic encapsulated. Note the bonding pad material is aluminum.

Shipping Method

Standard die carrier packages and wafer packages are vacuum-sealed with dessicant inside an ESD shielding moisture barrier bag. Sealed product is then placed inside corrugated cardboard box surrounded by bubble wrap or foam for maximum protection during shipment.

Figure 15. Die Pad Locations

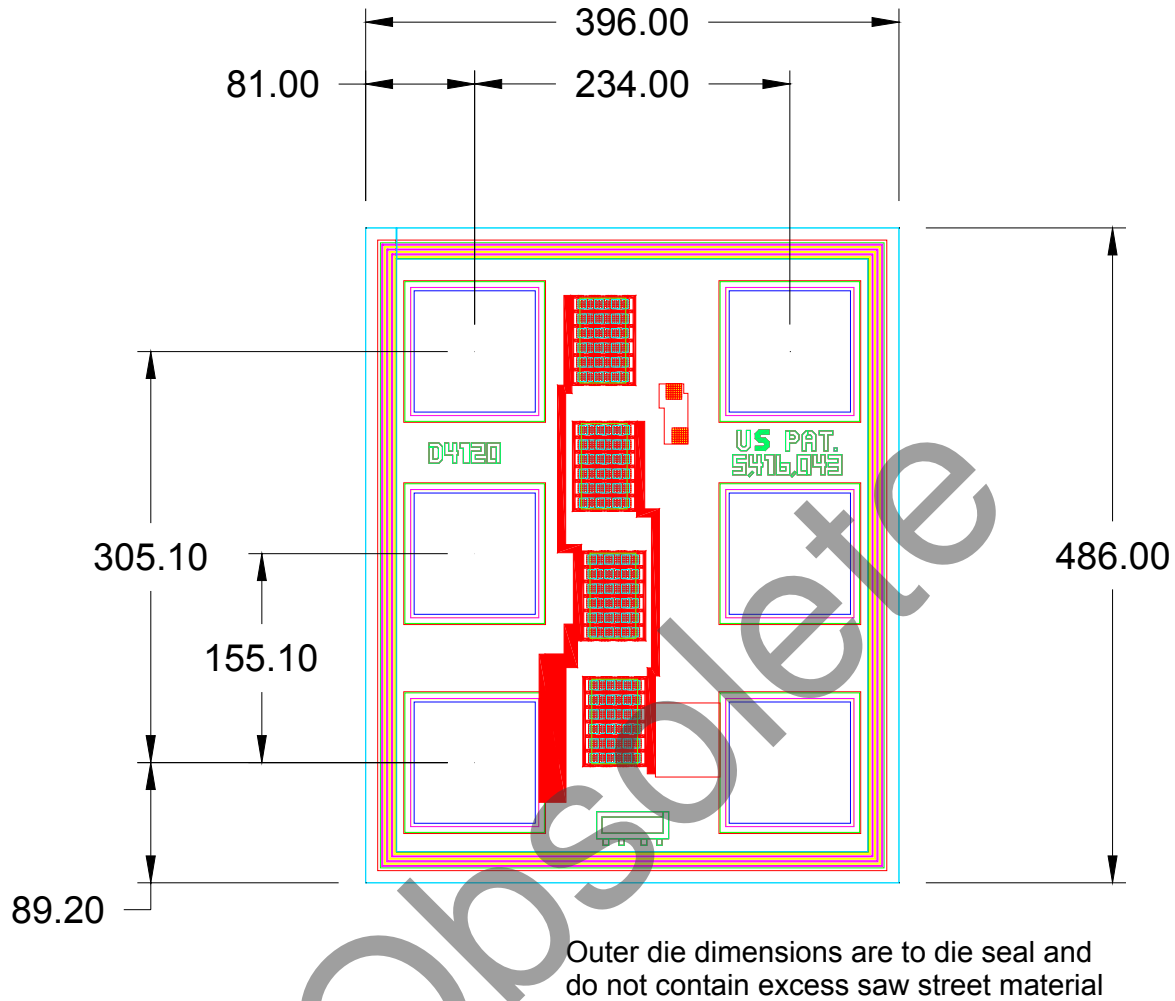


Table 6. Ordering Information

Order Code	Part Marking	Description	Package	Shipping Method
PE4120-90	D4120	PE4120-DIE-D	Blue Tape on Film Frame	Wafer / GDW Quantity
PE4120-99	D4120	PE4120-DIE-100W	Waffle Pack	100 units / Waffle Pack

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For a list of representatives in your area, please refer to our Web site at: <http://www.peregrine-semi.com>

Data Sheet Identification

Advance Information

The product is in a formative or design stage. The data sheet contains design target specifications for product development. Specifications and features may change in any manner without notice.

Preliminary Specification

The data sheet contains preliminary data. Additional data may be added at a later date. Peregrine reserves the right to change specifications at any time without notice in order to supply the best possible product.

Product Specification

The data sheet contains final data. In the event Peregrine decides to change the specifications, Peregrine will notify customers of the intended changes by issuing a PCN (Product Change Notice).

The information in this data sheet is believed to be reliable. However, Peregrine assumes no liability for the use of this information. Use shall be entirely at the user's own risk.

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Peregrine products are protected under one or more of the following U.S. patents: 6,090,648; 6,057,555; 5,973,382; 5,973,363; 5,930,638; 5,920,233; 5,895,957; 5,883,396; 5,864,162; 5,863,823; 5,861,336; 5,663,570; 5,610,790; 5,600,169; 5,596,205; 5,572,040; 5,492,857; 5,416,043. Other patents are pending.

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