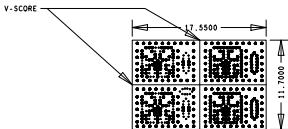
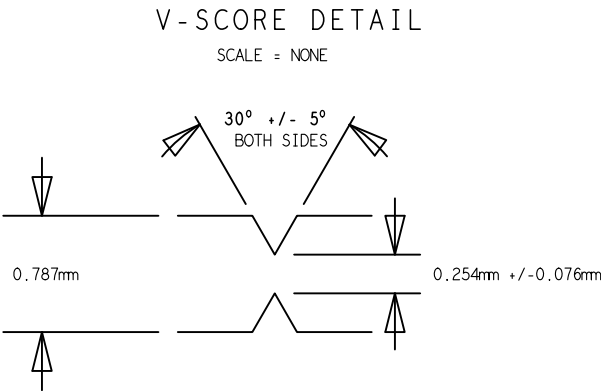


- NOTES: UNLESS OTHERWISE SPECIFIED, ALL DIMENSIONS ARE IN METRIC
1. INTERPRET DIMENSIONS AND TOLERANCES PER ANSI Y14.5M.
~~GERBER FILES CONTAIN BOARD OUTLINE FOR ALIGNMENT PURPOSES. REMOVE PRIOR TO FABRICATION.~~
 3. FABRICATE PCB PER IPC-6012, LATEST REVISION, TYPE 3, CLASS 2. THE DETAILED NOTES AND INSTRUCTIONS ON THIS DRAWING SUPERCEDE IPC REQUIREMENTS. BARE BOARD ACCEPTANCE PER IPC-A-600, LATEST REVISION.
 4. TRACE WIDTH/SPACE/VIA:
TRACE WIDTHS/SPACING TO BE WITHIN $\pm 20\%$ OF GERBER DATA.
MINIMUM TRACE WIDTH: OUTER LAYERS= $0.0852\text{mm} \pm 10\%$.
INNER LAYERS= NA $\pm 20\%$.
MINIMUM AIR GAP: OUTER LAYERS= $0.05592 \pm 20\%$.
INNER LAYERS= NA $\pm 20\%$.
MINIMUM VIA PAD DIAMETER: $0.10\text{mm} \pm 20\%$.
 5. MATERIAL:
NUMBER OF ELECTRICAL LAYERS IS 4.
MATERIALS AND OVERALL THICKNESS SEE STACKUP DETAIL.
LOAD BOARD AND PREPREG PER IPC-4101. COPPER FOIL PER IPC-MF-150.
MATERIAL'S GLASS TRANSITION TEMPERATURE (Tg) SHALL BE A MINIMUM OF 170° CENTIGRADE.
MATERIAL MUST MEET UL796 WITH A FLAMMABILITY RATING OF 94V-0
VENDOR UL LOGO AND DATE CODE TO BE SCREENED ON THE BOTTOM SIDE. IF NO BOTTOM SILKSCREEN PROVIDED VENDOR MAY ADD BOTTOM SILKSCREEN.
 6. TOLERANCES:
6A. LAYER TO LAYER REGISTRATION WITHIN $.076\text{mm}$.
6B. ALL HOLES TO BE LOCATED WITHIN $.076\text{mm}$ OF ORIGINAL CAD DATA.
6C. ALL HOLES SURROUNDED BY COPPER SHALL HAVE A MINIMUM ANNULAR RING OF $.076\text{mm}$.
6D. ALL PLATED THROUGH HOLES TO HAVE A MINIMUM $.015\text{mm}$ OF PLATING.
6E. HOLE DIMENSIONS AND TOLERANCES APPLY AFTER PLATING, SEE DRILL HOLE CHART.
6F. WARP AND TWIST NOT TO EXCEED $.254 \text{ MM/MM}$.
6G. CONDUCTOR WIDTHS/SPACINGS TO BE WITHIN $\pm 20\%$ OF GEBER DATA.
 7. PLATING OPTIONS: USE 7A
7A. 1Ag - IMMERSION SILVER 6-20 MICROINCHES MINIMUM PER IPC-4553.
~~7B. 0.20 µm OVER ELECTROLESS PALLADIUM OVER 0.3 µm OF PALLADIUM PER IPC-4552~~
~~7C. SELECTIVE HARD GOLD FINISH IN THE BUT AND POGPAD AREA(S). CLASS 1 50-100 MICROINCHES MICROINCHES THICK (MINOR HARDNESS 100-200) OVER NICKEL PLATE IN ACCORDANCE WITH IPC-A-600, LATEST REVISION, SECTION 1.8. CLASS 2 (200-300 MICROINCHES THICK).~~
~~7D. FABRICATE IN ACCORDANCE WITH IPC-6010. START WITH 17/121 COPPER~~
~~7E. HASL (NOT AIR COLDER LEVEL) BUT PADS MUST BE FLAT TO A MAX OF $.076\text{mm}$ (.003") ABOVE SURFACE. HASL FINISH TO BE USED ON TEST OR PROTOTYPE BOARDS ONLY. THIS FINISH DOES NOT COMPLY WITH ROHS DIRECTIVE.~~
 8. APPLY LPI (LIQUID PROTO-IMAGEABLE) SOLDERMASK OVER BARE COPPER (SMOBC) PER IPC-SM-840 CLASS "T" TO BOTH SIDES OF PCB. SOLDERMASK COLOR TO BE: GREEN
GERBER FILES REFLECT A ZERO OVERSIZE. VENDOR MAY OVERSIZE AS NEEDED, MAX THICKNESS $.015\text{mm}$. ~~IT IS NOT ACCEPTABLE FOR SOLDERMASK WEDDING TO DISAPPEAR BETWEEN FINE PITCH BALL PADS.~~
 9. APPLY SILKSCREEN LEGEND USING WHITE NON-CONDUCTIVE EPOXY INK. TRIM SILKSCREEN FROM ALL EXPOSED COPPER, TOP SIDE.
 10. VENDOR TO REMOVE NON-FUNCTIONAL PADS FROM INTERNAL LAYERS.
 11. VENDOR MAY ONLY ADD THIEVING OUTSIDE THE BOARD OUTLINE TO COMPENSATE FOR LOW COPPER DENSITY.
 12. REMOVE ALL BURRS AND BREAK SHARP EDGES, INSIDE CORNER MAXIMUM RADIUS 381mm.
 13. BARE BOARD ELECTRICAL TEST IS REQUIRED. USE THE SUPPLIED IPC-D-356 NETLIST "PRT-80235-01.IPC".
 14. MATRIX DRAWING: USE 14A
14A. NO MATRIX DRAWING IS REQUIRED. BOARDS TO BE DELIVERED FULLY ROUTED.
~~14B. MATRIX DRAWING PROVIDED. SEE FABRICATION DRAWING SHEET 2 OF 2.~~
~~14C. VENDOR TO GENERATE MATRIX DRAWING. VENDOR GENERATED MATRIX DRAWINGS REQUIRE APPROVAL BY PSEMI. PANELIZED BOARDS TO HAVE SAME ORIENTATION AND SHALL BE ROUTED AND RETAINED WITH BREAK AWAY TABS. SEE DETAIL D. SUPPORT RAIL WIDTH TO BE $0.33\text{mm} = 12.7\text{mm}$ WITH 1.52mm FIDUCIALS AND 0.178mm FIDUCIAL HOLES IN 3 CORNERS. PANELIZED SOLDERPASTE ORDER TO BE SUBMITTED TO PSEMI.~~
 15. PLANARITY: USE 15A,15B
15A. VARIATION OF BUMP PADS IN THE Z AXIS TO BE $\leq 5\mu\text{m}$.
15B. ALL VIAS TO BE NON-CONDUCTIVE EPOXY FILLED AND COPPER OVERPLATED AFTER PLATING AND BEFORE FINAL SURFACE FINISH. NON-CONDUCTIVE EPOXY (SAR E1 900 OR EQUIVALENT) IS RECOMMENDED. EPOXY SHALL NOT PROTRUDE FROM HOLES. THIS APPLIES TO ALL VIAS THAT ARE EXPOSED ON BOTH SIDES. A SMOOTH COPLANAR FINISH IS REQUIRED WHEN EXPOSED BY SOLDERMASK.
~~15C. ALL OTHER VIAS ARE TO BE PLUGGED AND FILLED WITH SOLDERMASK MATERIAL.~~
 16. CONTROLLED IMPEDANCE REQUIREMENTS: USE 16A
VENDOR MAY MODIFY DIELECTRIC THICKNESS BY 25% WITHOUT WRITTEN CONSENT. ANY MODIFICATION GREATER THAN 25% REQUIRES WRITTEN CONSENT FROM PSEMI.
16A. NO CONTROLLED IMPEDANCE MEASUREMENTS REQUIRED.
~~16B. VENDOR TO PROVIDE TEST COUPON AND IMPEDANCE REPORT.~~
~~0.157mm TRACES ON LAYER 1 ARE 50 OHMS, TRANSMISSION LINES N/A 10%.~~
~~0.157mm (.006") TRACES ON LAYER 1 ARE 50 OHMS, MICROSTRIP, 10%.~~
~~0.157mm (.006") TRACES ON LAYER 1 ARE 100 OHMS, DIFFERENTIAL, 10%.~~
 17. SHORTS DESIGNED IN BOARD: NO
NET XXXXXXXXXXXX.
~~NET XXXXXX TO GND, LAYER 1~~
 18. IPC-2221 TEST COUPONS A & B REQUIRED. TEST COUPONS SHALL BE IDENTIFIED AND TRACEABLE TO THE LOT. TEST COUPONS, DATA, CROSSECTIONS VERIFYING WIDTH AND CERTIFICATES OF CONFORMANCE SHALL ACCOMPANY ALL SHIPMENTS. MATERIAL VERIFICATION SHALL ALSO BE SENT IN WRITING. SHIPMENTS WITHOUT THESE CERTIFICATIONS WILL NOT BE ACCEPTED.
 19. DEVIATIONS BY FABRICATION FACILITY TO BE REPORTED TO PSEMI.

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DRILL CHART: TOP to LAYER_2				
ALL UNITS ARE IN MILLIMETERS				
FIGURE	FINISHED SIZE	TOLERANCE DRILL	PLATED	QTY
•	0.1	+0.0/-0.1	PLATED	70

DRILL CHART: TOP to BOTTOM				
ALL UNITS ARE IN MILLIMETERS				
FIGURE	FINISHED SIZE	TOLERANCE DRILL	PLATED	QTY
•	0.1016	+0.0/-0.1016	PLATED	438

DIMENSIONS IN mm/[Inches] TOLERANCES UNLESS OTHERWISE NOTED X.X = +/- .25/[-.1] X.XX = +/- .25/[-.01] X.XXX = +/- .127/[-.005] X.XXXX = +/- .0127/[-.0005] ANGLES = +/- 1/2 DEG	CONTRACT NO.		COMPANY	
	APPROVALS	DATE	TITLE	
MATERIAL	DRAWN R.MARROQUIN	07/08/21	PCB, PE42546 Shaggy Probe Board	
FINISH	CHECKED R.ALIDIO	07/08/21	SIZE B	RoHS COMPLIANCE RELEASE DATE
DO NOT SCALE DRAWING	ISSUED		DWG NO. PRT-80235	
	REVISIED BY		REV 01	
SCALE: NONE			SHEET: 1 of 1	

