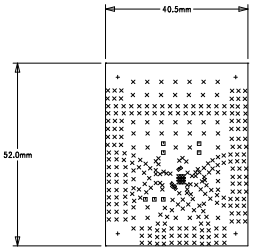
REVISIONS				
REV	ECN#	DESCRIPTION	DATE	APPROVED
03	SP808	REMOVED TOP SECTION	8-24-15	G. WU

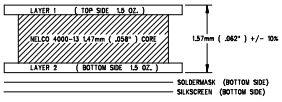
NOTES: UNLESS OTHERWISE SPECIFIED, ALL DIMENSIONS ARE IN METRIC

1. INTERPRET DIMENSIONS AND TOLERANCES PER ANSI Y14.5M.
2. GERBER FILES CONTAIN BOARD OUTLINE FOR ALIGNMENT PURPOSES, REMOVE PRIOR TO FABRICATION.
3. FABRICATION VENDOR MAY ADD _X_TEARDROPS, ___SOLDER TAILS TO PADS IN DUT AREA.
4. FABRICATE PCB PER IPC-6012, LATEST REVISION, TYPE 3, CLASS 2.
   THE DETAILED NOTES AND INSTRUCTIONS ON THIS DRAWING SUPERCEDE IPC REQUIREMENTS.
   BARE BOARD ACCEPTANCE PER IPC-A-600, LATEST REVISION.
5. NUMBER OF ELECTRICAL LAYERS IS "2". SEE LAYER STACKUP DETAIL FOR MATERIALS AND OVERALL THICKNESS.
   MINIMUM TRACE WIDTH FOR OUTER LAYERS = .28mm (.011") +/-20%, FOR INNER LAYERS = NA
   MINIMUM AIR GAP FOR OUTER LAYERS = .1524mm (.006") +/-20%, FOR INNER LAYERS = NA
   MINIMUM VIA PAD DIAMETER = .20mm (.008") +/-20%.
   ____ NOTE: THIS PCB HAS < .076mm (.003") TRACE/SPACE IN DUT AREA.
6. MATERIAL: LAMINATE AND PREPREG PER IPC-4101. COPPER FOIL PER IPC-MF-150.
   MINIMUM FINISHED EXTERNAL LAYER COPPER WEIGHT = ____1 OZ. _X_1.5 OZ. ___2 OZ. MINIMUM.
   MINIMUM INTERNAL LAYER COPPER WEIGHT = _X_0.5 OZ. ___ 1 OZ.
   THE MATERIAL'S GLASS TRANSITION TEMPERATURE (Tg) SHALL BE A MINIMUM OF 170 DEGREES CENTIGRADE.
   MATERIAL MUST MEET UL 796 WITH A FLAMMABILITY RATING OF 94V-0
   VENDOR'S UL LOGO AND DATE CODE TO BE SCREENED ON THE BOTTOM SIDE.
7. LAYER TO LAYER REGISTRATION WITHIN .076 (.003"). ALL HOLES TO BE LOCATED WITHIN .076mm (.003") OF ORIGINAL CAD DATA.
   ALL HOLES SURROUNDED BY COPPER LAND SHALL HAVE A MINIMUM ANNULAR RING OF .076mm (.003").
   ALL PLATED THROUGH HOLES TO HAVE A MINIMUM .025mm (.001") OF PLATING.
   HOLE DIMENSIONS AND TOLERANCES APPLY AFTER PLATING, SEE DRILL HOLE CHART.
   ___ .XX (XXX") VIAS MAY HAVE AN ANNULAR RING OF ZERO
8. PLATING OPTIONS:
   _X_ ENIG (ELECTROLESS NICKEL / IMMERSION GOLD) 2-10 MICROINCHES OF GOLD OVER A MINIMUM OF
   120 MICROINCHES OF NICKEL PER IPC-4552. THIS FINISH COMPLIES WITH RoHS DIRECTIVES.
   ___ SELECTIVE HARD GOLD FINISH IN THE DUT AND POGOPAD AREA(S).
   CLASS 1 50-100 MICROINCHES THICK (KNOOP HARDNESS 130-200) OVER NICKEL PLATE IN
   ACCORDANCE WITH IPC-A-600, LATEST REVISION, SECTION 4.0, CLASS 3 (200-800 MICROINCHES THICK).
   ___ HASL (HOT AIR SOLDER LEVEL) SMT PADS MUST BE FLAT TO A MAX OF .003" ABOVE SURFACE. HASL FINISH
   TO BE USED ON TEST OR PROTOTYPE BOARDS ONLY. THIS FINISH DOES NOT COMPLY WITH RoHS DIRECTIVES.
9. APPLY LPI (LIQUID PHOTO-IMAGEABLE) SOLDERMASK OVER BARE COPPER (SMOBC) PER IPC-SM-840 CLASS T
   TO BOTH SIDES OF PCB. SOLDERMASK COLOR TO BE: _X_GREEN ___BLUE ___RED ___CLEAR ___BLACK ___ORANGE.
   GERBER FILES REFLECT A ZERO OVERSIZE. FABRICATION VENDOR MAY OVERSIZE AS NEEDED, MAX THICKNESS .025mm (.001").
   IT IS ACCEPTABLE FOR SOLDERMASK WEBBING TO DISAPPEAR BETWEEN FINE PITCH BALL PADS.
10. APPLY SILKSCREEN LEGEND USING WHITE NON-CONDUCTIVE EPOXY INK. TRIM SILKSCREEN FROM ALL SOLDER PADS.
    ___TOP SIDE ONLY ___BOTTOM SIDE ONLY _X_BOTH SIDES
11. FABRICATION VENDOR MAY REMOVE NON-FUNCTIONAL PADS FROM INTERNAL LAYERS. FABRICATION VENDOR MAY
    ONLY ADD THIEVING OUTSIDE THE BOARD OUTLINE TO COMPENSATE FOR LOW COPPER DENSITY.
12. TOLERANCES: WARP AND TWIST NOT TO EXCEED .010 IN/IN, CONDUCTOR WIDTHS/SPACINGS TO BE WITHIN +/-20%
    OF GERBER DATA. REMOVE ALL BURRS AND BREAK SHARP EDGES, .381mm (.015") MAXIMUM. INSIDE CORNER MAXIMUM RADIUS
    _X_ NO MATRIX DRAWING IS REQUIRED. BOARDS TO BE DELIVERED FULLY ROUTED.
    ___ MATRIX DRAWING PROVIDED, SEE FABRICATION DRAWING SHEET 2 OF 2.
    ___ VENDOR TO GENERATE MATRIX DRAWING. VENDOR GENERATED MATRIX DRAWINGS REQUIRE APPROVAL BY PEREGRINE
    SEMICONDUCTOR. PANELIZED BOARDS TO HAVE SAME ORIENTATION AND SHALL BE ROUTED AND RETAINED WITH BREAK
    AWAY TABS. SEE DETAIL B. SUPPORT RAIL WIDTH TO BE 6.35mm (.25") - 12.7mm (.50") WITH
    1.52mm (.060") FIDUCIALS AND 3.175mm (.123") TOOLING HOLES IN 3 CORNERS
    PANELIZED SOLDERPASTE GERBER TO BE SUBMITTED TO PEREGRINE SEMICONDUCTOR.
13. PLANARITY:
    ____ VARIATION OF BUMP PADS IN THE Z AXIS TO BE <=5um.
    _X_ ALL 0.25mm (.010") VIAS TO BE EPOXY FILLED AFTER PLATING AND BEFORE FINAL SURFACE FINISH.
    NON-CONDUCTIVE EPOXY (SAN_EI 900 OR EQUIVALENT) IS RECOMMENDED.
    EPOXY SHALL NOT PROTRUDE FROM HOLES. THIS APPLIES TO ALL VIAS THAT ARE EXPOSED ON BOTH SIDES.
    A SMOOTH COPLANAR FINISH IS REQUIRED WHEN EXPOSED BY SOLDERMASK.
    _X_ ALL OTHER VIAS ARE TO BE PLUGGED AND FILLED WITH SOLDERMASK MATERIAL.
14. BARE BOARD ELECTRICAL TEST IS REQUIRED. USE THE SUPPLIED IPC-D-356 NETLIST "PRT-60631-03.IPC".
15. CONTROLLED IMPEDANCE REQUIREMENTS: FABRICATION VENDOR MAY MODIFY DIELECTRIC THICKNESS BY 25% WITHOUT
    WRITTEN CONSENT. ANY MODIFICATION GREATER THAN 25% REQUIRES WRITTEN CONSENT FROM PEREGRINE SEMICONDUCTOR.
    ___ NO CONTROLLED IMPEDANCE MEASUREMENTS REQUIRED.
    _X_ VENDOR TO PROVIDE TEST COUPON AND IMPEDANCE REPORT.
    0.805mm (.0317") TRACES ON LAYER 1 ARE 50 OHMS, CO-PLANAR TRANSMISSION LINE +/- 10%.
    0.279mm (.011") TRACES ON LAYER 1 ARE 100 OHMS, DIFFERENTIAL TRANSMISSION LINE +/- 10%.
    IPC-2221 TEST COUPONS A & B REQUIRED. TEST COUPONS SHALL BE IDENTIFIED AND TRACEABLE TO THE LOT.
    TEST COUPONS, DATA, CROSSECTIONS OF IMPEDANCE TRACES VERIFYING WIDTH AND CERTIFICATES OF CONFORMANCE
    SHALL ACCOMPANY ALL SHIPMENTS.
16. OPEN DESIGNED IN BOARD: _X_ NO ___ YES



SIZE	QTY	SYM	PLATED	TOL
4	4	+	YES	+/-0.0762
0.35	302	X	YES	+0/-0.35
0.9398	7	□	YES	+/-0.0762
0.2	6	◇	YES	+0/-0.20
0.25	9	⧖	YES	+0/-0.25

2 LAYER STACK-UP DETAIL



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DIMENSIONS IN mm/[inches]
TOLERANCES UNLESS OTHERWISE NOTED
X.X = +/- .2.5/[.1]
X.XX = +/- .25/[.01]
X.XXX = +/- .127/[.005]
X.XXXX = +/- .0127/[.0005]
ANGLES = +/- 1/2°

PCB DESIGNER: R.Marroquin	DATE: 05-26-2015
ELECTRICAL ENGINEER: G.Wu	DATE: 05-26-2015
PROJECT MANAGER	DATE

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FABRICATION DRAWING
PE4152 EVK

SIZE	RoHS COMPLIANCE	DRAWING NO.	REV
B	4-24-06 (Pb)	PRT-60631	03

SCALE: 1/1 | PADS FILENAME: PRT-60631-02 | SHEET 1 of 1