PE42443

Document Category: Product Specification

UltraCMOS SP4T RF Switch, 1.8 GHz–5 GHz

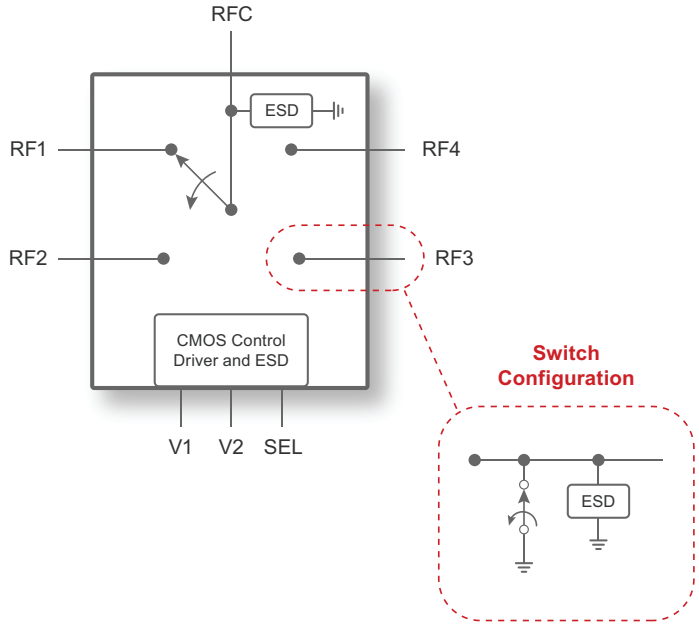
Features

- Low insertion loss:
  - 0.4 dB at 2.6 GHz typical
  - 0.49 dB at 3.8 GHz typical
- High linearity IIP3: 85 dBm
- High power handling: 40 dBm RMS, 50 dBm peak
- 105 °C operating temperature
- Packaging — 20-lead 4 x 4 mm LGA

Applications

- Analog hybrid beamforming RF front end
- 5G massive MIMO active antenna system (AAS)
- 4G/4.5G TD-LTE macro/micro cell/RRH

Figure 1 ▪ PE42443 Functional Diagram



Product Description

The PE42443 is a HaRP™ technology-enhanced SP4T RF switch that supports a frequency range from 1.8 GHz to 5 GHz. It delivers extremely low insertion loss, high linearity and fast switching time with high input power handling capability making this device ideal for hybrid beamforming and in 5G massive MIMO (multi-input multi-output) applications. No blocking capacitors are required if DC voltage is not present on the RF ports.

pSemi's HaRP™ technology enhancements deliver high linearity and excellent harmonics performance. It is an innovative feature of the UltraCMOS® process, offering the performance of GaAs with the economy and integration of conventional CMOS.

The PE42443 is manufactured on pSemi's UltraCMOS process, a patented advanced form of silicon-on-insulator (SOI) technology.

Revision History

Table 1 ▪ Revision History

Document Revision	Date	Change Description
DOC-106518-7	April 2024	Table 4, Electrical Specifications.

Absolute Maximum Ratings

Exceeding absolute maximum ratings listed in **Table 2** may cause permanent damage. Operation should be restricted to the limits in **Table 3**. Operation between operating range maximum and absolute maximum for extended periods may reduce reliability.

ESD Precautions

When handling this UltraCMOS device, observe the same precautions as with any other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rating specified in **Table 2**.

Latch-up Immunity

Unlike conventional CMOS devices, UltraCMOS devices are immune to latch-up.

Table 2 ▪ Absolute Maximum Ratings for PE42443

Parameter/Condition	Min	Max	Unit
VDD Positive Supply Voltage	-0.3	5.5	V
Digital Input Voltage	-0.3	3.6	V
RF Input Power, RMS		41	dBm
RF Input Power, Peak		51	dBm
RF Input Power, RMS (2s Survivability)(1)		43.5	dBm
Storage Temperature	-65	150	°C
ESD Voltage HBM(2)		1000	V
ESD Voltages, CDM(3)		500	V

Notes:

1) The part was tested at 43.5 dBm average power / 50.5 dBm peak power for two seconds with 100 exposures with a cool down period of five seconds between each exposure. This test was conducted at 115 °C T_{CASE}. Signal type: LTE TDD, ETM1.1 test model, 10 ms frame duration, 70% duty cycle.
2) Human body model (MIL-STD 883 Method 3015).
3) Charged device model (JEDEC JESD22-C101).

Recommended Operating Conditions

Table 3 lists the recommending operating conditions for the PE42443. Devices should not be operated outside the operating conditions listed below.

Table 3 ▪ Recommended Operating Conditions for PE42443

Parameter	Min	Typ	Max	Unit
VDD Positive Supply Voltage	4.5	5	5.50	V
VSS Negative Supply Voltage (External VSS Applied)	-3.4	-3.3	-3.2	V
IDD Positive Supply Current		135	200	µA
ISS Negative Supply Current		1	25	µA
Control Voltage High	1.17		3.60	V
Control Voltage Low	-0.30		0.60	V
Digital Input Leakage Current			10	µA
Temperature Range	-40	25	105	°C

Electrical Specifications

Table 4 provides the PE42443 key electrical specifications at +25 °C T_{CASE}, VDD = 5V (ZS = ZL = 50Ω), unless otherwise specified.

Table 4 ▪ PE42443 Electrical Specifications

Parameter	Condition	Min	Typ	Max	Unit
Insertion Loss	1800 MHz		0.33	0.40	dB
	2700 MHz		0.40	0.45	dB
	3800 MHz		0.49	0.59	dB
	5000 MHz		0.65	0.74	dB
Return Loss Input/Output	1800–2300 MHz		37		dB
	2300–3300 MHz		27		dB
	3300–3800 MHz		24		dB
	3800–5000 MHz		24		dB
Isolation	Isolation requirement valid for RFC to RFx ports and RFx to RFx ports. 1800 to 2300 MHz.	33	34		dB
	Isolation requirement valid for RFC to RFx ports and RFx to RFx ports. 2300 to 3300 MHz.	30	32		dB
	Isolation requirement valid for RFC to RFx ports and RFx to RFx ports. 3300 to 3800 MHz.	29	28		dB
	Isolation requirement valid for RFC to RFx ports and RFx to RFx ports. 3800 to 5000 MHz.	26	27		dB
IMD3 (CW)	Measured using two pulsed CW (3.5 GHz, 2.5% duty cycle for 4.616 msec period), each 34 dBm. Measurement bandwidth: 100 kHz for carriers and intermodulation products. Spec. limit valid within theoretical IMD3 center frequency ± 10 MHz. Carrier spacings: 50 MHz, 100 MHz.		-103	-100	dBc
IMD3 (LTE)	LTE signal EMT1.1 34 dBm, 8 dB PAR @ 3500 MHz		-101	-99	dBc
Input IP3 (LTE)	LTE signal EMT1.1 34 dBm, 8 dB PAR @ 3500 MHz	84	85		dBm
Input IP3 (CW)	Measured using 2x 34 dBm CW signals, tone spacings 50 MHz, 100 MHz	83	85		dBm
Input IP2 (CW)		139	140		dBm
Input Power Handling (RMS)[1]	During static operation, no hot switching. Input signal is LTE 10 MHz ETM1.1 carrier with 10 dB PAR. No compression expected at peak power.			40	dBm
Input Power Handling (Peak)				50	dBm
Input Power Handling (RMS)	During transition phase (hot switching). Input signal is LTE 10 MHz ETM1.1 carrier with 8 dB PAR.			39	dBm
Input Power Handling (Peak)				47	dBm

Table 4 ▪ PE42443 Electrical Specifications

Parameter	Condition	Min	Typ	Max	Unit
Reflected Power Handling (RMS)	Max 10s time duration. Input signal is 37 dBm LTE 10 MHz ETM1.1 carrier with 8 dB PAR on 3.5:1 VSWR. Simultaneous presence of forward and reflected signal. To be tested with different phases of the reflected signal at the output of DUT. Reflected power.			32	dBm
Reflected Power Handling (Peak)				40	dBm
Reflected Power Handling (RMS)	Indefinite time duration. Input signal is 37 dBm LTE 10 MHz ETM1.1carrier with 8 dB PAR on 2:1 VSWR. Simultaneous presence of forward and reflected signal. To be tested with different phases of the reflected signal at the output of DUT.			27	dBm
Reflected Power Handling (Peak)				35	dBm
Settling Time[2]	Insertion loss settled to final value +- 0.1 dB. Small signal test.		1	1.1	µsec
Switching Time	50% Vctrl to gain settled to IL +/- 0.5 dB. Small signal test.		0.82	0.86	µsec
Switching Interval	Time allowed between switching events.		16		µsec
Input P0.1dB[3]	P0.1dB peak using LTE_TDD_10M at 3400 MHz with 10 dB PAR	50.2	50.5		dBm
Second Harmonic	Input signal CW signal of 35 dBm @ 3.5 GHz		-109	-99	dBc
Third Harmonic	Input signal CW signal of 37 dBm @ 2.5 GHz		-107	-103	dBc
Relative Phase Variation between Paths[4]	Relative phase variation between the two phase shifter paths (Path1/2: RF1 - RF4 and Path3/4: RF2 - RF3) at 3.8 GHz			1.66	degree
	Relative phase variation between the two phase shifter paths (Path1/2: RF1 - RF4 and Path3/4: RF2 - RF3) at 5 GHz			2.23	degree
Phase Delay	RFC to RF1/4 at 3.8 GHz	50.6	53	56	degree
	RFC to RF2/3 at 3.8 GHz	56.4	59	62	degree

Notes:

1) The input power handling (RMS) needs to be de-rated to 39 dBm for 105 °C T_{CASE} operation to maintain safe operation over the lifetime of the part.
2) At 1.1 µsec after an switching event, the third harmonic on the selected port should settle to -70 dBc, for an input signal with peak power of 43 dBm or less.
3) The P0.1dB is measured under steady state condition and not 1.1 µs after a switching event.
4) The phase shifter paths are shown in **Figure 13**. The 'relative phase variation' is calculated with between Path1 and Path3 (or Path2 and Path4). The reason for choosing this combination is because RF1 and RF4 are symmetric ports (and so are RF2 and RF3), so the phase error between Path1 and Path2 (or Path3 and Path4) should be negligible.

SP4T Control Logic

Table 5 provides the control logic truth table for the PE42443.

Table 5 ▪ Truth Table for PE42443

ON Port	V2	V1	SEL
RF1	0	0	0
RF2	0	1	0
RF3	1	0	0
RF4	1	1	0
Transpose			
RF1	1	1	1 or no-connect
RF2	1	0	1 or no-connect
RF3	0	1	1 or no-connect
RF4	0	0	1 or no-connect

Typical Performance Data

Figure 2–Figure 10 show the typical performance data at +25 °C T_{CASE}, VDD = 5V (ZS = ZL = 50Ω), unless otherwise specified.

Figure 2 ▪ Insertion Loss RFC to RFx vs. Frequency

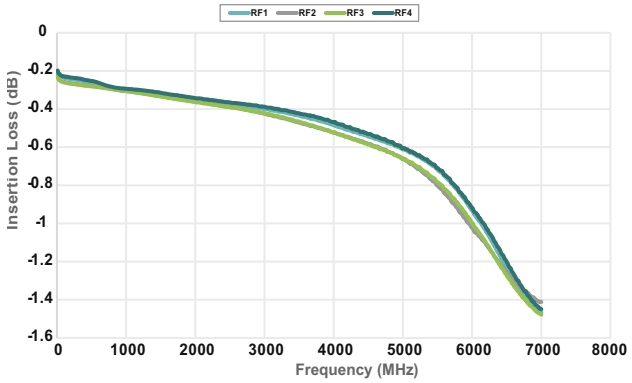


Figure 3 ▪ Insertion Loss RF1 Over Temperature

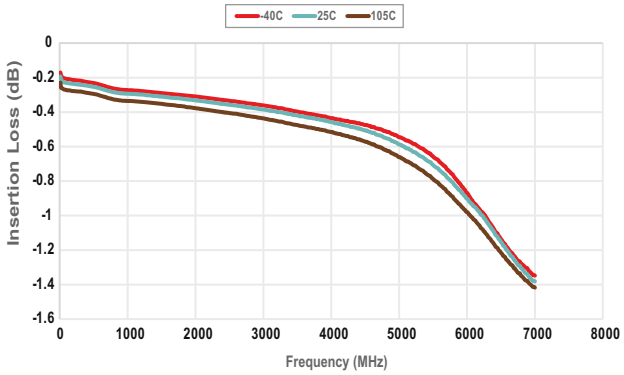


Figure 4 ▪ Input Return Loss When RFx Is On

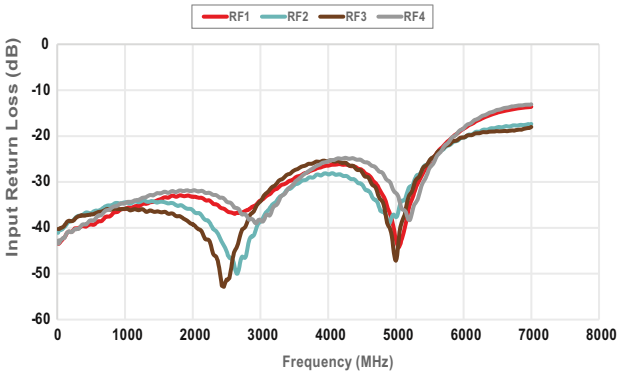


Figure 5 ▪ Return Loss When RFx Is Selected

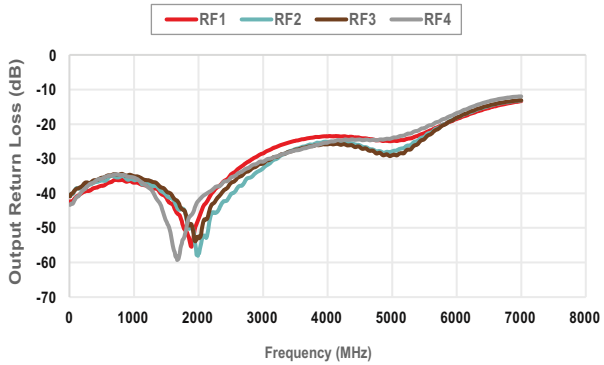


Figure 6 ▪ Return Loss When RFx Is Not Selected

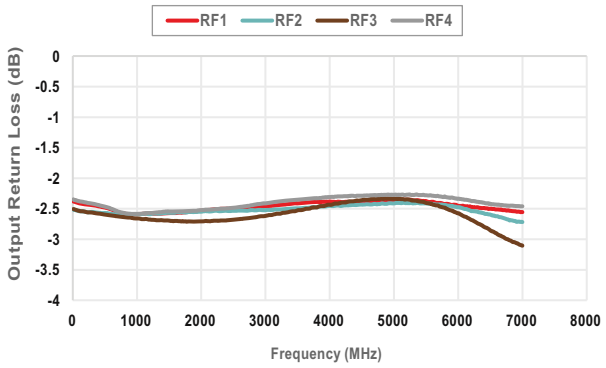


Figure 7 ▪ Isolation When RF1 Is On

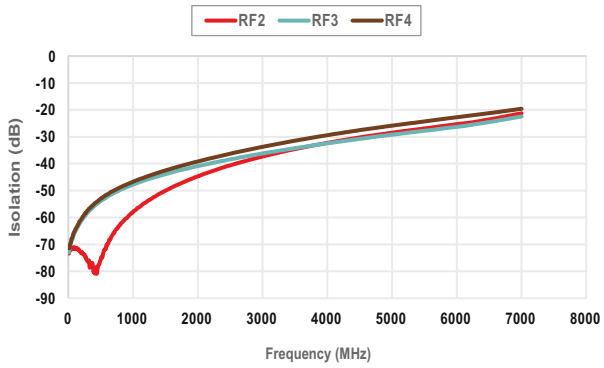


Figure 8 ▪ Isolation When RF2 Is On

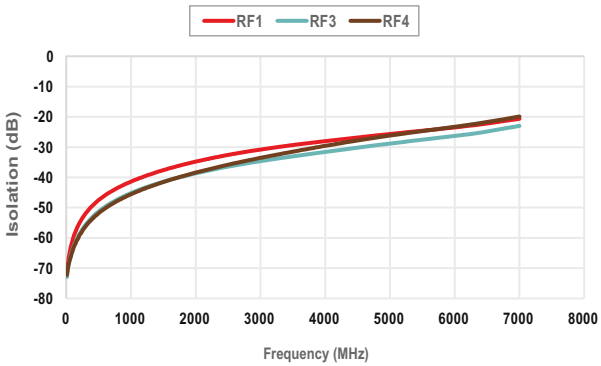


Figure 9 ▪ Isolation When RF3 Is On

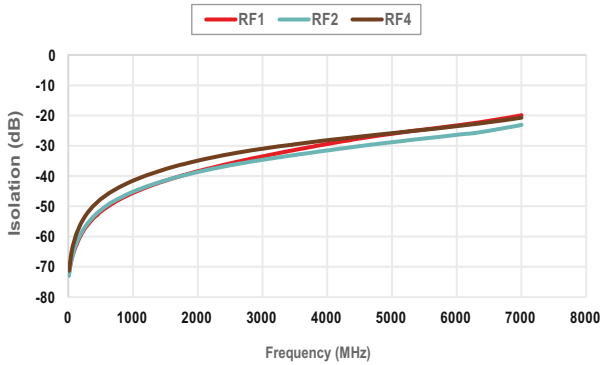
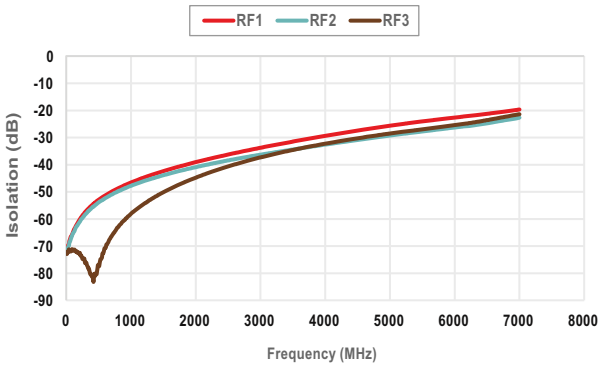


Figure 10 ▪ Isolation When RF4 Is On



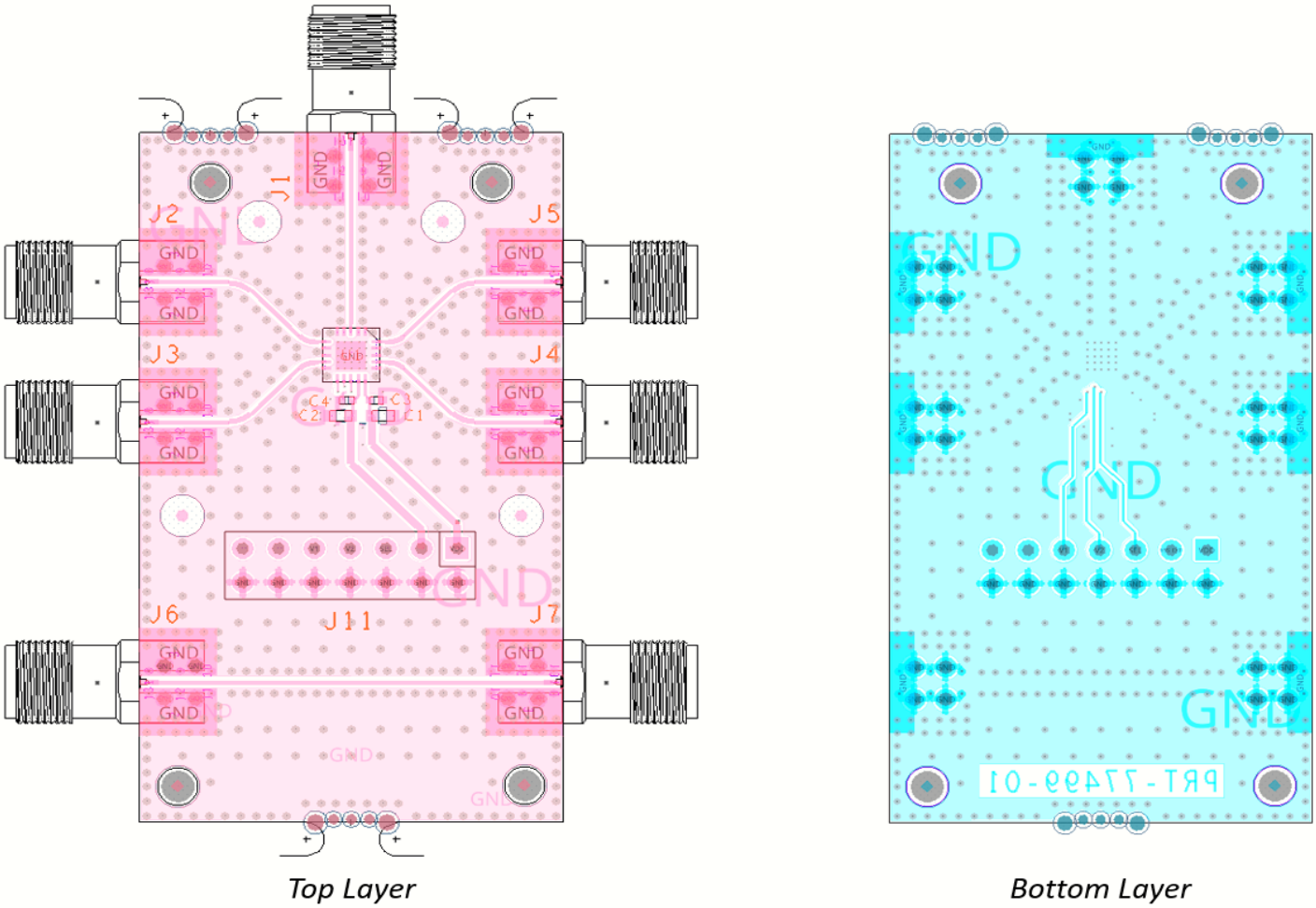
Evaluation Kit

The SPDT switch evaluation board (PRT-77499) was designed to ease customer evaluation of pSemi's PE42443. The RF common port is connected through a 50Ω transmission line via the top SMA connector J1. RF1, RF2, RF3 and RF4 are connected through 50Ω transmission lines via side SMA connectors J2, J3, J4 and J5, respectively. A through 50Ω transmission is available via SMA connectors J6 and J7. This transmission line can be used to estimate the loss of the PCB over the environmental conditions being evaluated.

The EVK board is constructed with four metal layers on dielectric materials of Rogers 4003C™ and FR406 with a total thickness of 62 mils. Layer 1 and layer 3 provide ground for the 50Ω transmission lines. The 50Ω transmission lines are designed in layer 1 and use a coplanar waveguide design with a trace width of 15.8 mils, signal-to-ground spacing of 8 mils and trace metal thickness of 1.7 mils. The board stackup for 50Ω transmission lines has 8 mil thickness of Rogers 4003C between layer 1 and layer 2, and 42 mil thickness of FR406 between layer 2 and layer 3.

Please consult manufacturers' guidelines for proper board material properties in your application. The PCB should be designed in such a way that RF transmission lines and sensitive DC I/O traces such as VSS_EXT are heavily isolated from one another; otherwise, the true performance of the PE42443 will not be yielded.

Figure 11 ▪ Evaluation Board Layout, Top/Bottom Layer for PE42443



Top Layer *Bottom Layer*

Evaluation Board Schematic and BOM

Figure 12 shows the evaluation board schematic. Table 6 shows the evaluation board bill of materials.

Figure 12 ▪ PE42443 Evaluation Board Schematic

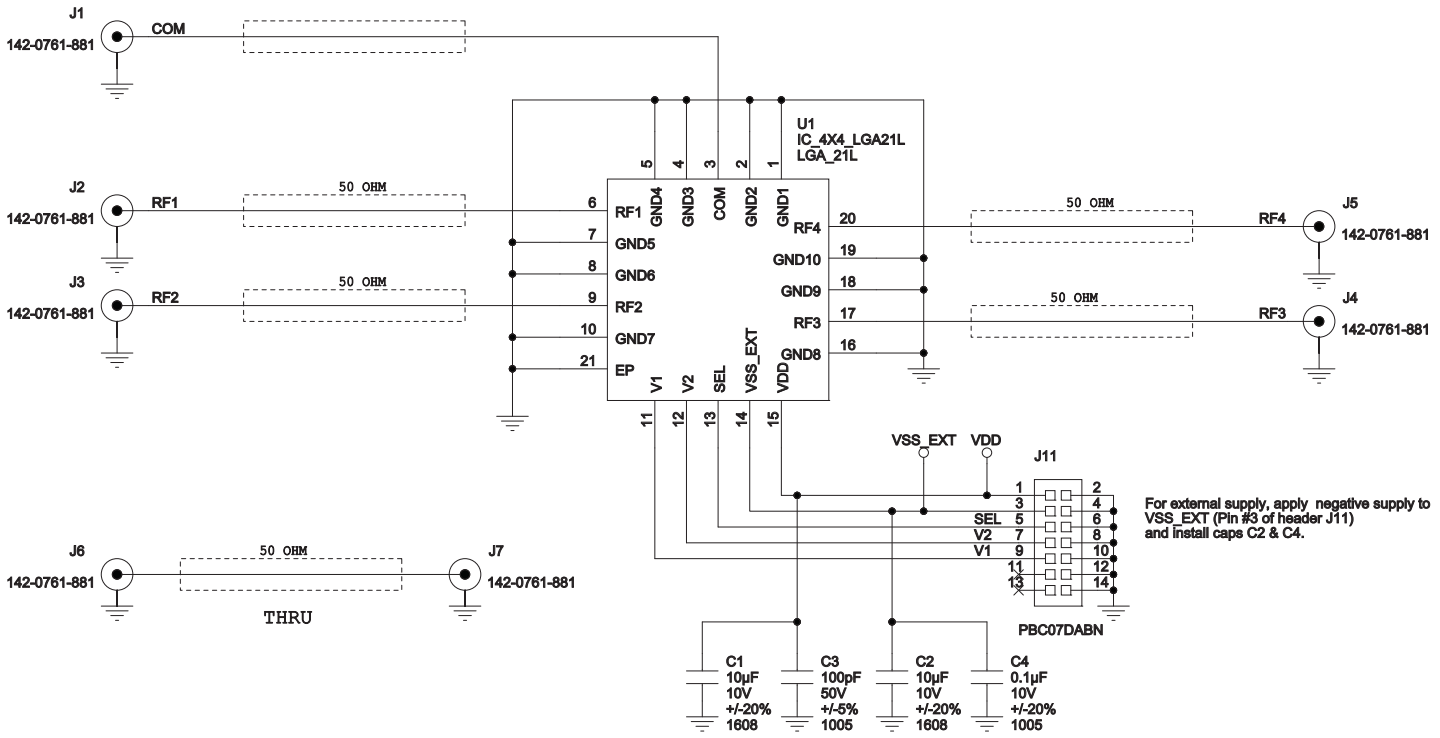


Table 6 ▪ PE42443 Evaluation Board BOM Components

Reference	Value	Description	Manufacturer	Mfg. Part Number
C1,C2	10 µF	CAP, SMD, CER, 10 µF, 10V, +/-20%, X7T, 0603 (1608 Metric)	Murata Electronics North America	GRM188D71A106-MA73D
C3	100 pF	CAP, SMD, CER, 100 pF, 50V, +/-5%, C0G, NP0, 0402 (1005 Metric)	Murata Electronics North America	GRM1555C1H101-JA01D
C4	0.1 µF	CAP, SMD, CER, 0.1 µF, 10V, +/-20%, X5R, 0402 (1005 Metric)	Murata Electronics North America	GRM155R61A104-MA01D
J1,J2,J3,J4,J5, J6,J7	142-0761-881	CONN, Coaxial Connectors (RF), SMA, SMD, Jack, Female Socket, 50 Ohm	Cinch Connectivity Solutions Johnson	142-0761-881
J11	PBC07DABN	CONN, Rectangular Connectors - Headers, Male Pins, Header Unshrouded Breakaway, TH, Male	Sullins Connector Solutions	PBC07DABN
PCB1	PCB	PCB,PE42444 SP4T EVK	pSemi Corporation	PRT-77499
U1	IC-4X4_L-GA21L			

Application Diagram

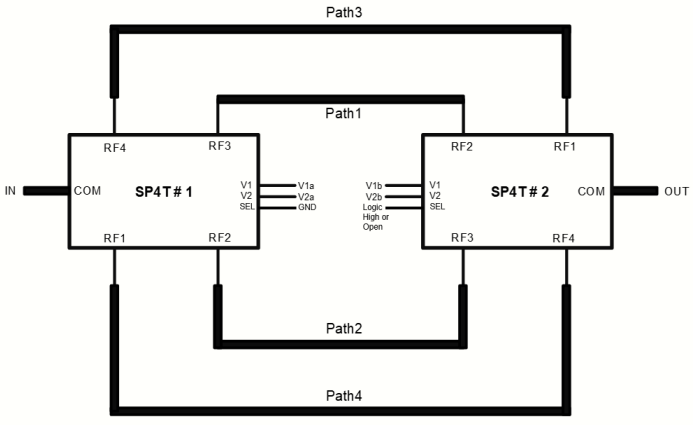
Table 7 ▪ Lookup Table for Application Diagram

Phase State	ON Ports		Path
	SP4T #1	SP4T #2	
State 1	RF3	RF2	Path 1
State 2	RF2	RF3	Path 2
State 3	RF4	RF1	Path 3
State 4	RF1	RF4	Path 4

Figure 13 shows an application diagram for a phase shifter application implemented using two SP4T switches.

Note: To characterize the parameters Relative Phase, Relative Phase Error and Relative Phase Variation between Paths, all four paths had exactly the same delay line lengths.

Figure 13 ▪ Application Diagram for PE42443 Used in a Phase Shifter



Pin Information

This section provides pinout information for the PE42443. **Figure 14** shows the pin map of this device for the available package. **Table 8** provides a description for each pin.

Figure 14 ▪ Pin Configuration (Top View)

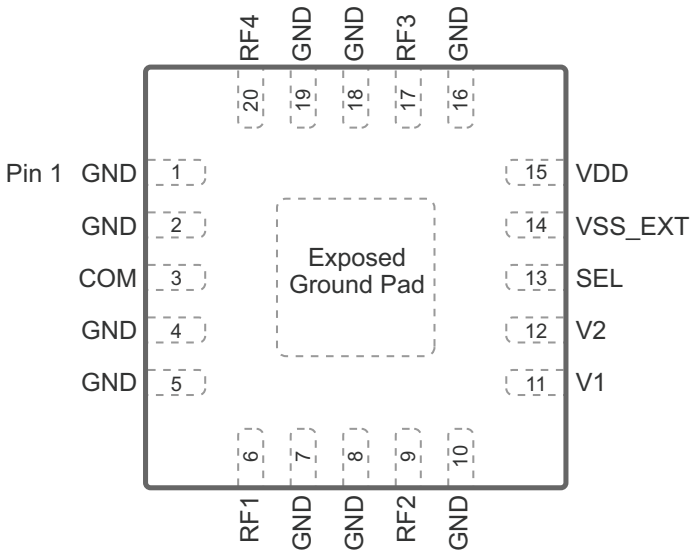


Table 8 ▪ Pin Descriptions for PE42443

Pin No.	Pin Name	Description
1	GND	Ground
2	GND	Ground
3	COM[1]	RF common port
4	GND	Ground
5	GND	Ground
6	RF1[1]	RF port 1
7	GND	Ground
8	GND	Ground
9	RF2[1]	RF port 2
10	GND	Ground
11	V1	Digital control logic input 1
12	V2	Digital control logic input 2
13	SEL[2]	Logic select—used to determine definition for V1 and V2 pins

Table 8 ▪ Pin Descriptions for PE42443 (Cont.)

Pin No.	Pin Name	Description
14	VSS_EXT	External negative supply
15	VDD	Supply voltage
16	GND	Ground
17	RF3[1]	RF port 3
18	GND	Ground
19	GND	Ground
20	RF4[1]	RF port 4
Pad	GND	Exposed pad: ground for proper operation.

1) RF pins 3, 6, 9, 17 and 20 must be at 0 V DC. The RF pins do not require DC blocking capacitors for proper operation if the 0 V DC requirement is met.
2) Internal pull-up resistor will set pin to logic high if pin is floating. Ground pin to set to logic low.

Packaging Information

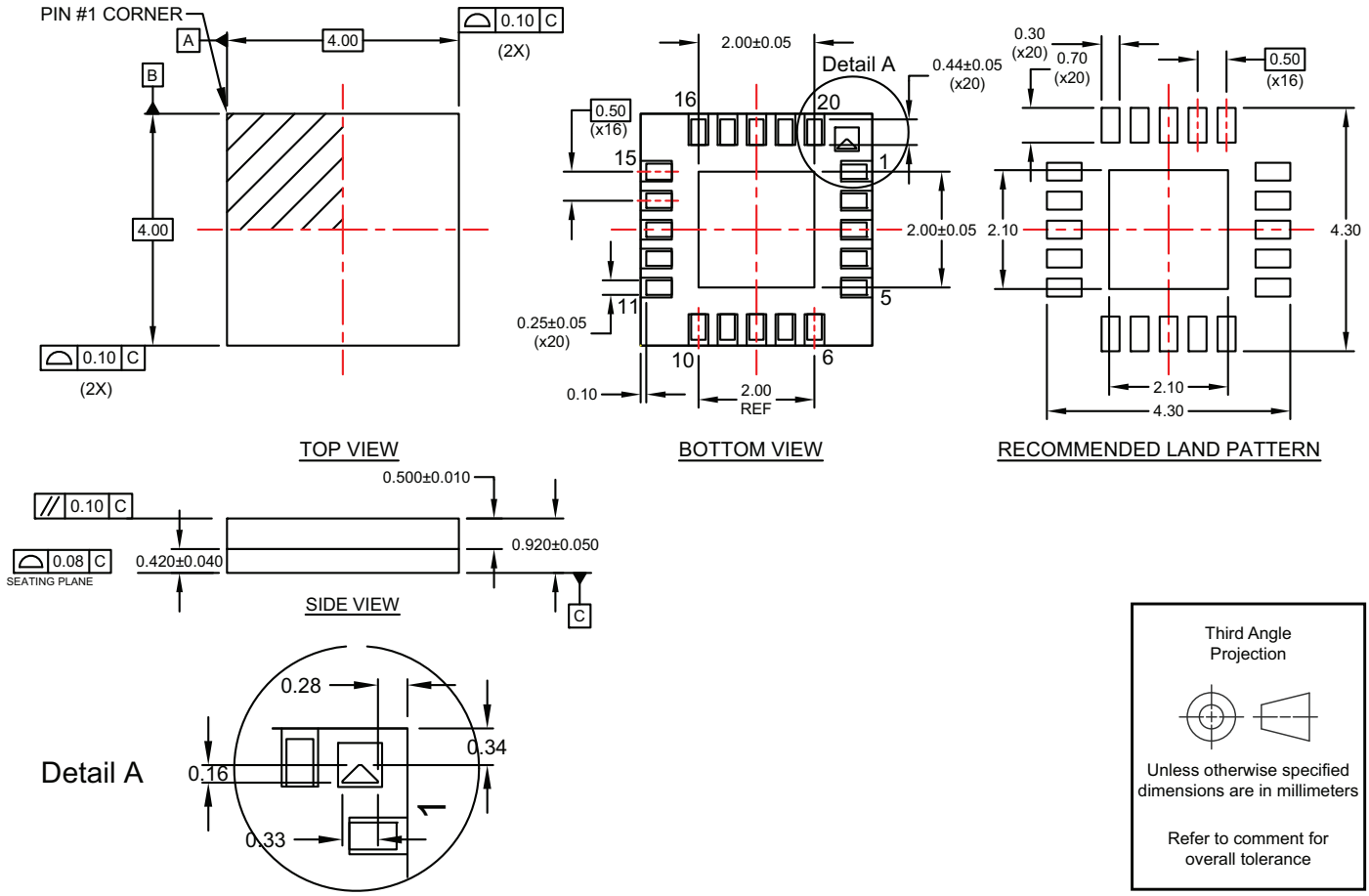
This section provides packaging data including the moisture sensitivity level, package drawing, package marking and tape-and-reel information.

Moisture Sensitivity Level

The moisture sensitivity level rating for the PE42443 in the 20-lead 4 x 4 mm LGA package is MSL 3.

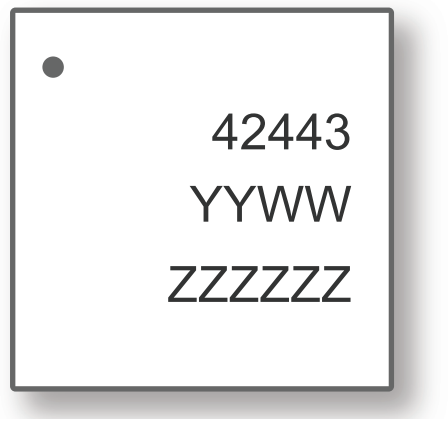
Package Drawing

Figure 15 ▪ Package Mechanical Drawing for 20-lead 4 x 4 mm LGA



Top-Marking Specification

Figure 16 ▪ Package Marking Specifications for PE42443

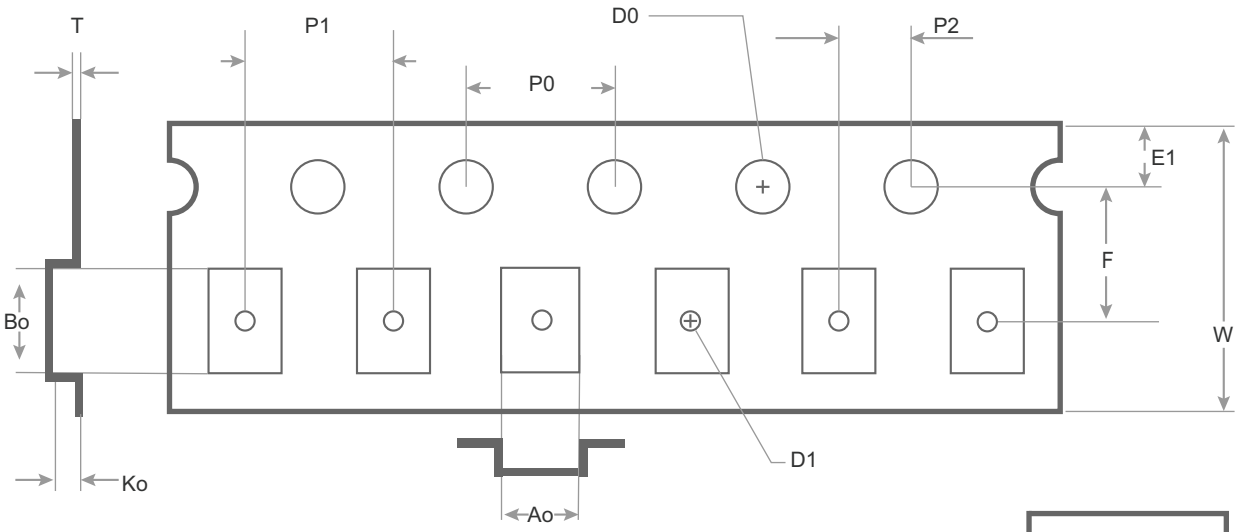


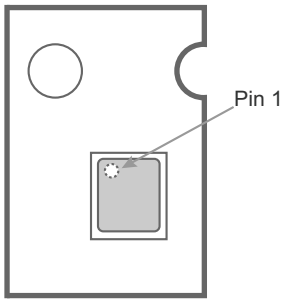
● = Pin 1 indicator
42443 = Product part number
YY = Last two digits of assembly year (2022 = 22)
WW = Work week of assembly lot start date (01, ..., 52)
ZZZZZZ = Assembly lot code (max six characters)

DOC-100702-1

Tape and Reel Specification

Figure 17 ▪ Tape and Reel Specifications for 20-lead 4 x 4 mm LGA





Device Orientation in Tape

Notes:

Not drawn to scale.
Dimensions are in millimeters.
Maximum cavity angle 5 degrees.
Bumped die are oriented active side down.

Carrier Tape Dimension Table

Pocket	Nominal	Tolerance	Pocket	Nominal	Tolerance
Ao	4.30	+/-0.1	D1	1.50	+0.2/-0.0
Bo	4.30	+/-0.1	D0	1.50	+0.1/-0.0
Ko	1.25	+/-0.1	E1	1.75	+/-0.1
P1	8.00	+/-0.1	P0	4.0	+/-0.1
W	12.00	+0.3/-0.1	P2	2.0	+/-0.05
F	5.50	+/-0.05	T	0.30	+/-0.03

Ordering Information

Table 9 lists the available ordering codes for the PE42443 as well as available shipping methods.

Table 9 ▪ Order Codes for PE42443

Order Codes	Description	Packaging	Shipping Method
PE42443A-Z	PE42443 SP4T switch	Green 20-lead 4 x 4 mm LGA	3000 units/T&R
EK42443-01	PE42443 evaluation kit	Evaluation kit	1/box

Document Categories

Advance Information

The product is in a formative or design stage. The datasheet contains design target specifications for product development. Specifications and features may change in any manner without notice.

Preliminary Specification

The datasheet contains preliminary data. Additional data may be added at a later date. pSemi reserves the right to change specifications at any time without notice in order to supply the best possible product.

Product Specification

The datasheet contains final data. In the event pSemi decides to change the specifications, pSemi will notify customers of the intended changes by issuing a CNF (Customer Notification Form).

Product Brief

This document contains a shortened version of the datasheet. For the full datasheet, contact sales@psemi.com.

Sales Contact

For additional information, contact Sales at sales@psemi.com.

Disclaimers

The information in this document is believed to be reliable. However, pSemi assumes no liability for the use of this information. Use shall be entirely at the user's own risk. No patent rights or licenses to any circuits described in this document are implied or granted to any third party. pSemi's products are not designed or intended for use in devices or systems intended for surgical implant, or in other applications intended to support or sustain life, or in any application in which the failure of the pSemi product could create a situation in which personal injury or death might occur. pSemi assumes no liability for damages, including consequential or incidental damages, arising out of the use of its products in such applications.

Patent Statement

pSemi products are protected under one or more of the following U.S. patents: patents.psemi.com

Copyright and Trademark